

## Input Range Synchronous Buck Controller

## Features

- Wide Input Voltage Range: 8V ~ 30V
- Up to 93% Efficiency
- No Loop Compensation Required
- Dual-channeling CC/CV control
- Cable drop Compensation from 0Ω to 0.3Ω
- Programmable CC Current
- Thermal Shutdown
- Over current protection
- UVLO protection
- Available in SOP8-PP Package

## Applications

- Car Charger / Adaptor
- LED Driver
- Pre-Regulator for Linear Re
- Distributed Power Systems
- Battery Charger

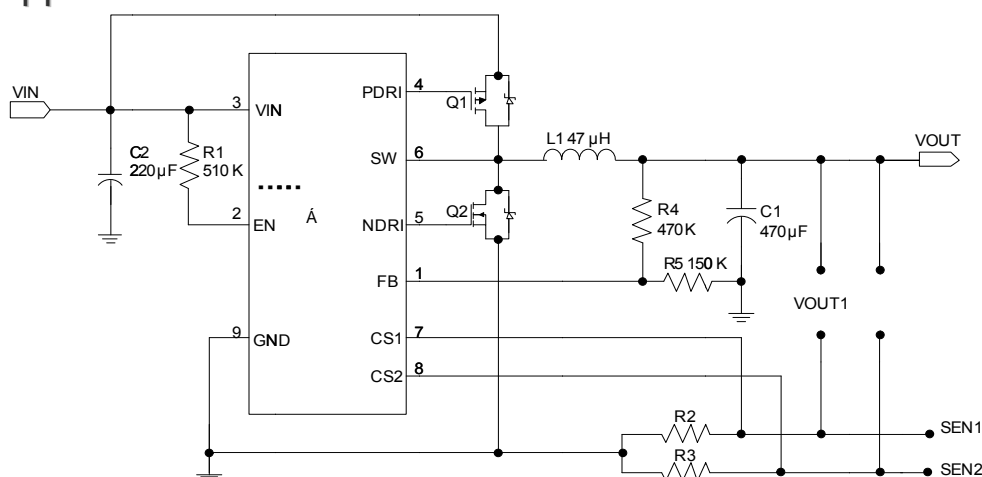
## Description

The **HM511J** is a wide input range step down DC/DC converter from a high voltage input supply. Operating with an input voltage range of 8V ~ 30V, the **HM511J** achieves 4.2A continuous output current with excellent load and line regulation. The synchronous architecture provides for highly efficient designs. Constant current and constant voltage mode operation provide fast transient response and eases loop stabilization.

The **HMFI1J6** features a dual-channeling CV/CC mode control functions. It operates in the Constant output Current mode or Constant output Voltage mode. The over current protection current value is set by current sensing resistors.

The HMF11J requires a minimum number of readily available standard external components. Other features include cable drop compensation, and thermal sh

## Typical Application Circuit

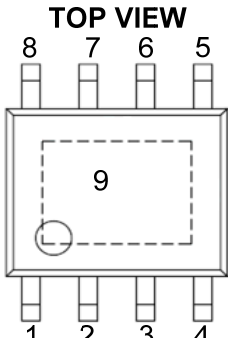


\*The output voltage is set by R4 and R5:  $V_{OUT} = 1.21V \cdot [1 + (R4/ R5)]$ .

\*The output current of VOUT1 is set by  $I_{CS1}=100\text{mv}/R2$ .

\*The output current of VOUT2 is set by R2  $I_{CS2}=100\text{mv}/R3$ .

## Pin Assignment and Description

|  <p><b>TOP VIEW</b></p> <p>8 7 6 5</p> <p>1 2 3 4</p> <p><b>SOP8-PP(Exposed Pad)</b><br/>*The exposed pad (Pin 9) must be soldered to a large PCB.</p> | PIN | NAME | DESCRIPTION                  |
|---|-----|------|------------------------------|
|   | 1   | FB   | Feedback                     |
|   | 2   | EN   | ON/OFF Control (High Enable) |
|   | 3   | VIN  | Input Supply Voltage         |
|   | 4   | PDRI | PMOS Gate Drive              |
|   | 5   | NDRI | NMOS Gate Drive              |
|   | 6   | SW   | Switch Node                  |
|   | 7   | CS1  | Current Sense Input1         |
|   | 8   | CS2  | Current Sense Input2         |
|   | 9   | GND  | Ground                       |

## Absolute Maximum Ratings (Note 1)

- Input Supply Voltage ..... - 0.3V ~ 35V
- PDRI PIN Voltage..... - 0.3V ~ 35V
- EN, FB, NDRI Voltages..... - 0.3V ~ 6V
- SW Voltage ..... - 0.3V ~ (VIN + 1V)
- Operating Temperature Range(Note 2)..... -40°C ~ +85°C
- Junction Temperature..... +150°C
- Storage Temperature Range..... - 65°C ~ +150°C
- Lead Temperature (Soldering, 10 sec)..... +265°C

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** The HT FI Ì J is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

## Pin Functions

**FB (Pin 1):** Feedback Pin. Receive the feedback voltage from an external resistive divider across the output. The output voltage is set by R1 and R2:  $V_{OUT} = 1.21V \cdot [1 + (R4 / R5)]$ .

**EN (Pin 2):** En Control Input. Forcing this pin above 0.9V enables the part. Forcing this pin below 0.6V shutting down the device. Do not leave EN floating.

**VIN (Pin 3):** Main power supply Pin.

**PDRI (Pin 4):** The drive for the high-side P-channel MOSFET switch.

**NDRI (Pin 5):** The drive for the low-side N-channel MOSFET switch.

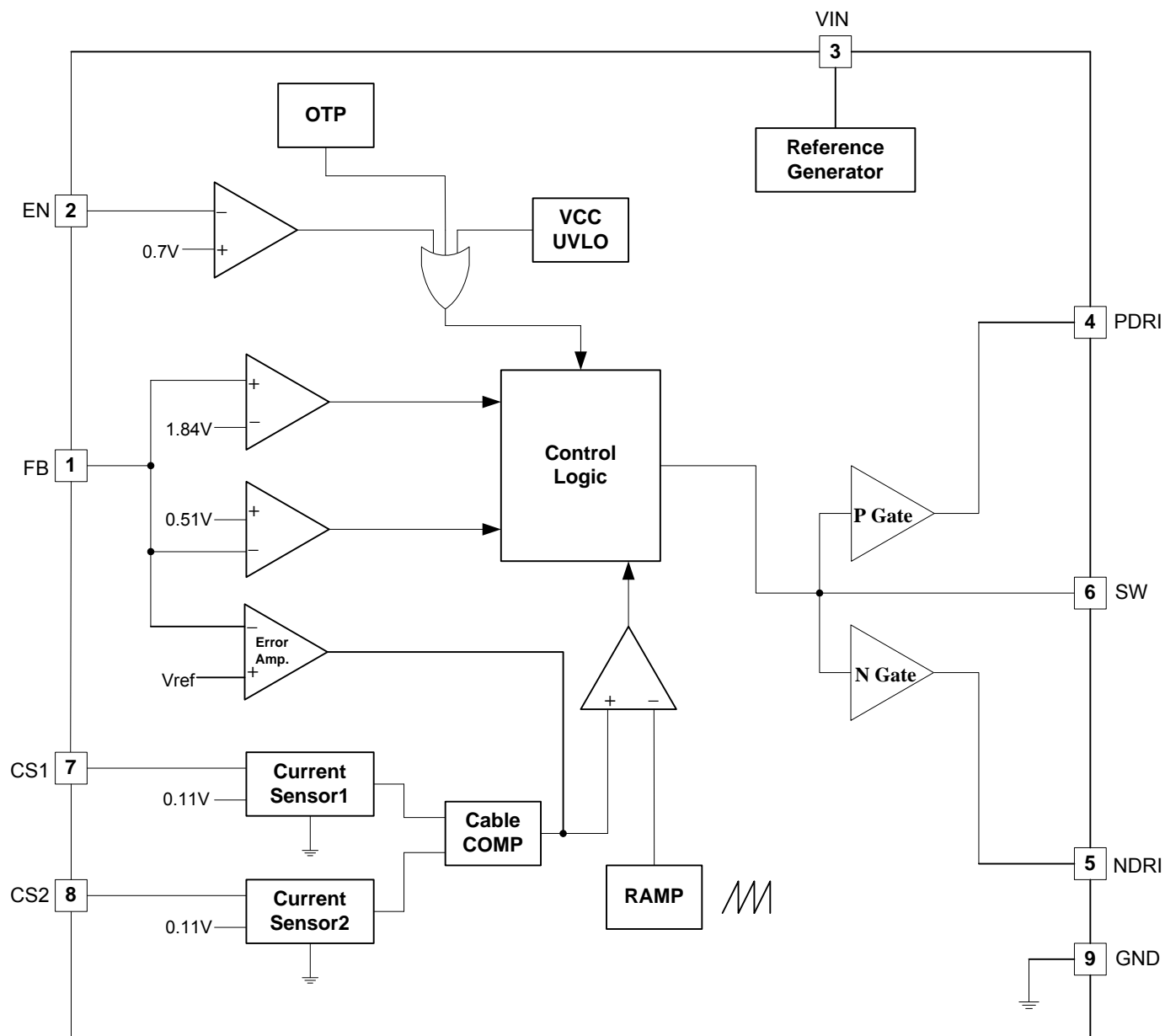
**SW (Pin 6):** Switch Node.

**CS1 (Pin 7):** Current or voltage sense pin of VOUT1. If SEN1 is larger than the sense voltage, the HT FI Ì J will shut down for protection. The output current is programmed by connecting a resistor, R2. The output current is set by R2:  $I_{CS1} = 100\text{mv} / R2$ .

**CS2 (Pin 8):** Current or voltage sense pin of VOUT2. If SEN2 is larger than the sense voltage, the HT FI Ì J will shut down for protection. The output current is programmed by connecting a resistor, R3. The output current is set by R3  $I_{CS1} = 100\text{mv} / R3$ .

**GND (Pin 9):** Ground Pin.

## Block Diagram



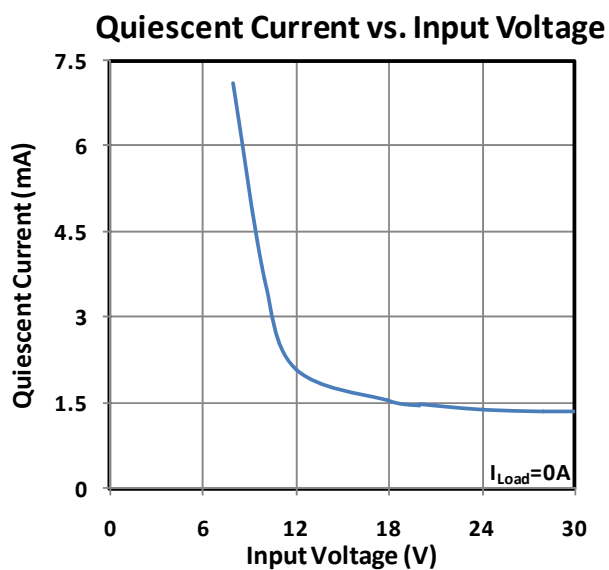
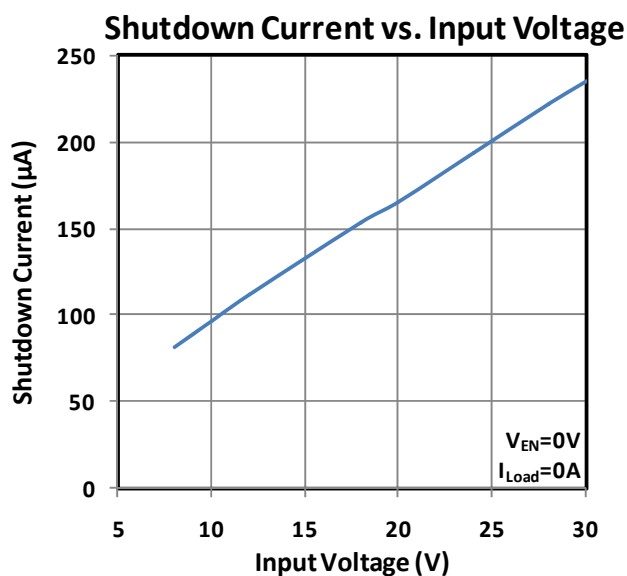
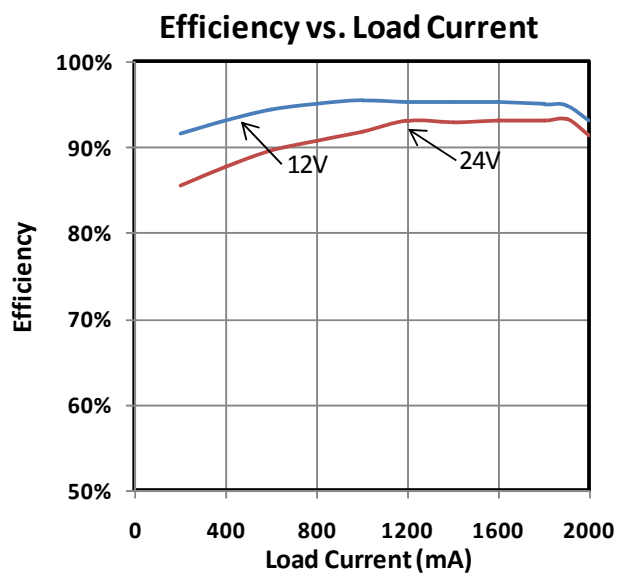
## Electrical Characteristics

Operating Conditions: TA=25℃, VIN = 12V, R4 = 33K, R5 = 10K, unless otherwise specified.

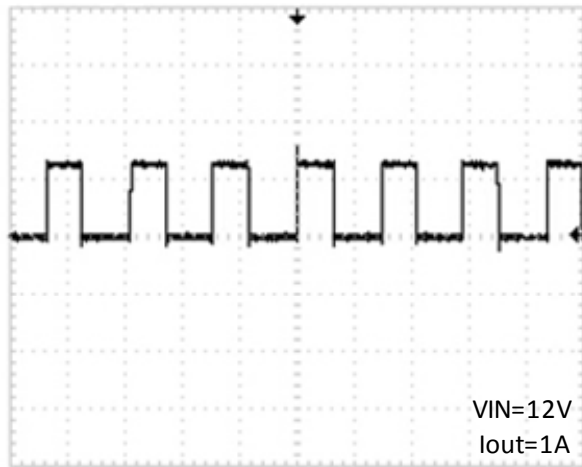
| SYMBOL       | PARAMETER                                 | CONDITIONS | MIN  | TYP      | MAX  | UNITS |
|--------------|---|------------|------|----------|------|-------|
| VIN          | Operating Voltage Range                   |            | 8    |          | 30   | V     |
| IQ           | Quiescent Current                         | VIN = 12V  |      | 2        |      | mA    |
| IOFF         | Shutdown Current                          | VEN = 0V   |      | 112      |      | μA    |
| VUVLO        | Input UVLO Threshold                      |            |      | 4.35     |      | V     |
| ΔVUVLO       | UVLO Hysteresis                           |            |      | 200      |      | mV    |
| VOVLO        | OVLO Threshold                            |            |      | 31.5     |      | V     |
| ΔVOVLO       | OVLO Hysteresis                           |            |      | 2.5      |      | V     |
| VFB          | Regulated Voltage                         |            | 1.17 | 1.21     | 1.25 | V     |
| ΔVFB         | Regulated Voltage Tolerance               |            | -2   |          | +2   | %     |
| IFB          | Feedback Pin Input Current                |            |      |          | 0.05 | μA    |
| Vcs1<br>Vcs2 | Reference Voltage Of<br>Current Sense Pin |            | 90   | 100      | 110  | mV    |
| fOSC         | Oscillator Frequency Range                |            | 100  | 130      | 150  | kHz   |
| fOSC-SHORT   | Short-Circuit Frequency                   |            |      | 0.1*fOSC |      | kHz   |
| DC           | Max Duty Cycle                            |            |      |          | 100  | %     |
| VEN          | EN Falling Threshold                      |            | 0.6  | 0.7      | 0.9  | V     |
| IEN          | EN Bias Current                           | VEN=1V     |      | 0.2      | 1    | μA    |
| TSD          | Thermal Shutdown                          |            |      | 145      |      | ℃     |
| TRSD         | Thermal Shutdown<br>Recovery              |            |      | 100      |      | ℃     |

## Typical Performance Characteristics

Operating Conditions:  $T_A=25^{\circ}\text{C}$ , unless otherwise specified.

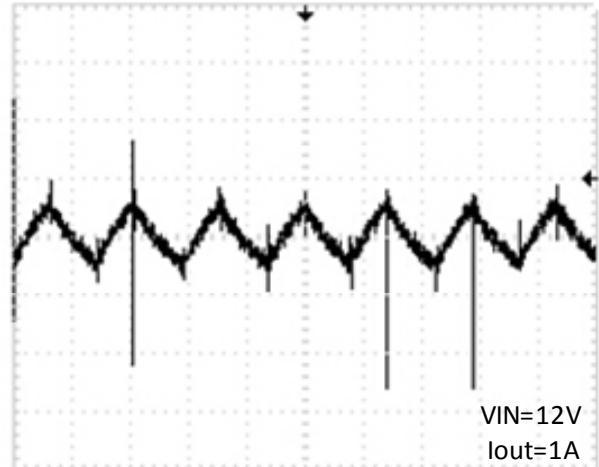


SW Ripple



10V/div  
 5 μs/div

Output Ripple



200mV/div  
 5 μs/div

## Application Information

The HT FI Ĩ J operates by a constant frequency, current mode architecture. The output voltage is set by an external divider returned to the FB pin. An error amplifier compares the divided output voltage with a reference voltage of 1.21V and adjusts the peak inductor current accordingly.

### Dual-channeling CV/CC mode control

HT FI Ĩ J provides the function of dual-channeling CV/CC mode control. The constant output current control mode and constant output voltage control mode. CS pins are connected to the current sensing resistors to prevent the condition of output short circuit and output over current.

### Thermal Protection

The total power dissipation in HT FI Ĩ J is limited by a thermal protection circuit. When the device temperature rises to approximately +145°C, this circuit turns off the output, allowing the IC to cool. The thermal protection circuit can protect the device from being damaged by overheating in the event of fault conditions. Continuously running the HT FI Ĩ J into thermal shutdown degrades device reliability.

### Output Cable Resistance Compensation

To compensate for resistive voltage drop across the charger's output cable, the HT FI Ĩ J integrates a simple, user-programmable cable voltage drop compensation using the impedance at the FB pin. Choose the proper feedback resistance values for cable compensation. The delta VOUT voltage rises when the feedback resistance R5 value rises. The delta VOUT voltage rises when the feedback resistance R3 value rises, use the equation below:

$$V_{OUT} = \left(1 + \frac{R4}{R5}\right) \times V_{FB} + R4 \times \frac{V_{Rsense}}{100mV} \times 2.5\mu A$$

### Setting Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. It is recommended to use divider resistors with 1% tolerance or better. To improve efficiency at very light loads consider using larger value resistors. If the values are too high the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable. For most applications, a resistor in the 10kΩ to 1MΩ range is suggested for R5. R4 is then given by:

$$R4 = R5 \cdot [(V_{OUT} / V_{REF}) - 1]$$

where VREF is 1.21V.

### Inductor Selection

For most applications, the value of the inductor will fall in the range of 4.7μH to 47μH. Its value is chosen based on the desired ripple current. Large value inductors lower ripple current and small value inductors result in higher ripple currents. Higher VIN or VOUT also increases the ripple current as shown in equation. A reasonable starting point for setting ripple current is ΔIL = 1680mA (40% of 4.2A).

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the



ripple current to prevent core saturation. Thus, a 5.88A rated inductor should be enough for most applications (4.2A +1680mA). For better efficiency, choose a low DC-resistance inductor.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or perm alloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs. size requirements and any radiated field/EMI requirements than on what the HT FI Ì J requires to operate.

### Output and Input Capacitor Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle  $V_{OUT}/V_{IN}$ . To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ required } I_{RMS} \cong I_{OMAX} \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{1/2}}{V_{IN}}$$

This formula has a maximum at  $V_{IN} = 2V_{OUT}$ , where  $I_{RMS} = I_{OUT}/2$ . This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

The selection of  $C_{OUT}$  is driven by the required effective series resistance (ESR). Typically, once the ESR requirement for  $C_{OUT}$  has been met, the RMS current rating generally far exceeds the  $I_{RIPPLE(P-P)}$  requirement. The output ripple  $\Delta V_{OUT}$  is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left( ESR + \frac{1}{8fC_{OUT}} \right)$$

Where  $f$  = operating frequency,  $C_{OUT}$  = output capacitance and  $\Delta I_L$  = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since  $\Delta I_L$  increases with input voltage.

Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum. These are specially constructed and tested for low ESR so they give the lowest ESR for a given volume.

### Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as: Efficiency = 100% - (L1+ L2+ L3+ ...) where L1, L2, etc. are the individual losses as a percentage of input power. Although all

dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: VIN quiescent current and  $I^2R$  losses. The VIN quiescent current loss dominates the efficiency loss at very low load currents whereas the  $I^2R$  loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The VIN quiescent current is due to two components: the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge  $\Delta Q$  moves from VIN to ground. The resulting  $\Delta Q/\Delta t$  is the current out of VIN that is typically larger than the DC bias current. In continuous mode,  $I_{GATECHG} = f(Q_T + Q_B)$  where  $Q_T$  and  $Q_B$  are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to VIN and thus their effects will be more pronounced at higher supply voltages.

2.  $I^2R$  losses are calculated from the resistances of the internal switches,  $R_{SW}$  and external inductor  $R_L$ . In continuous mode the average output current flowing through inductor L is “chopped” between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a

function of both top and bottom MOSFET  $R_{DS(ON)}$  and the duty cycle (DC) as follows:  $R_{SW} = R_{DS(ON)TOP} \times DC + R_{DS(ON)BOT} \times (1-DC)$  The  $R_{DS(ON)}$  for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain  $I^2R$  losses, simply add  $R_{SW}$  to  $R_L$  and multiply the result by the square of the average output current. Other losses including  $C_{IN}$  and  $C_{OUT}$  ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

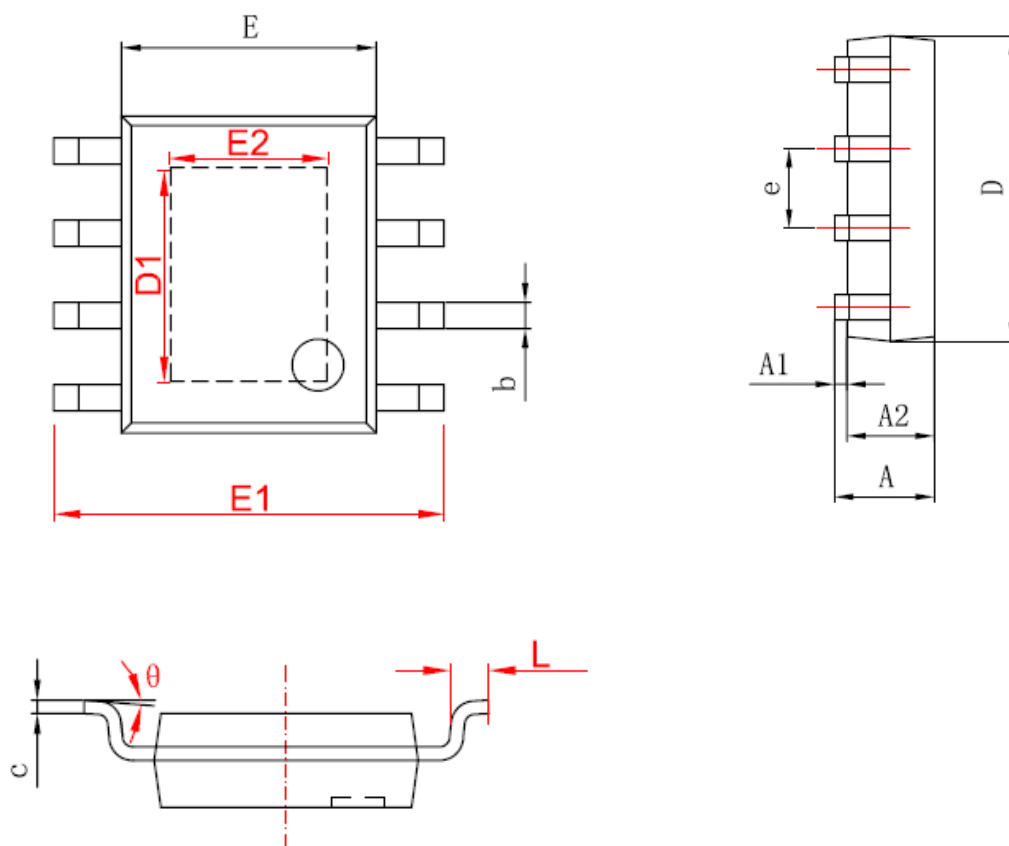
### Board Layout Suggestions

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the HT FI Ì J. Check the following in your layout.

1. The power traces, consisting of the GND trace, the SW trace and the VIN trace should be kept short, direct and wide.
2. Put the input capacitor as close as possible to the device pins (VIN and GND).
3. SW node is with high frequency voltage swing and should be kept small area. Keep analog components away from SW node to prevent stray capacitive noise pick-up.
4. Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacitors.

## Packaging Information

### SOP8-PP (EXP PAD) Package Outline Dimension



| Symbol   | Dimensions In Millimeters |       | Dimensions In Inches |       |
|----------|---------------------------|-------|----------------------|-------|
|          | Min                       | Max   | Min                  | Max   |
| A        | 1.350                     | 1.750 | 0.053                | 0.069 |
| A1       | 0.050                     | 0.150 | 0.004                | 0.010 |
| A2       | 1.350                     | 1.550 | 0.053                | 0.061 |
| b        | 0.330                     | 0.510 | 0.013                | 0.020 |
| c        | 0.170                     | 0.250 | 0.006                | 0.010 |
| D        | 4.700                     | 5.100 | 0.185                | 0.200 |
| D1       | 3.202                     | 3.402 | 0.126                | 0.134 |
| E        | 3.800                     | 4.000 | 0.150                | 0.157 |
| E1       | 5.800                     | 6.200 | 0.228                | 0.244 |
| E2       | 2.313                     | 2.513 | 0.091                | 0.099 |
| e        | 1.270(BSC)                |       | 0.050(BSC)           |       |
| L        | 0.400                     | 1.270 | 0.016                | 0.050 |
| $\theta$ | 0°                        | 8°    | 0°                   | 8°    |