HM1493

Wide Range Synchronous Buck Controller for QC2.0

Feature

- Wide Input Voltage Range: 10V to 30V
- Up to 93% Efficiency
- CC/CV Mode Control
- Fixed switching frequency 130kHZ
- Internal QC2.0 Fast Charging Function
- Supports Quick Charge 2.0 specification
- Class A: 5V/9V/12V Output Voltage
- Meet Chinese Telecommunication Industrial Standard YD/T 1591-2009
- Support USB DCP applying 2.7V on DP line and 2.7V on DM line
- Support USB DCP applying 1.2V on DP line and DM line
- Automatic selection of DP/DM mode for an at attached device
- Complaint with Apple and Samsung devices
- Thermal Shutdown
- Short Circuit Protect, Over Current Protect
- UVLO, OVLO
- Available in SOP-8L Package

Description

The HM1493 is a synchronous buck controller with a fast charge protocol controller, and follows Quick Charge 2.0 specification.

HM1493 can operating with an input voltage range from 10V to 30V, the HM1493 achieves 2.5A continuous output current with excellent load and line regulation. The switching frequency is fixed 130kHz.

HM1493 can support the full output voltage range of Class A. It also can support USB BC compliant device, Apple/Samsung devices and automatically detects whether a connected powered device is Quick Charge 2.0 capable before enabling output voltage adjustment.

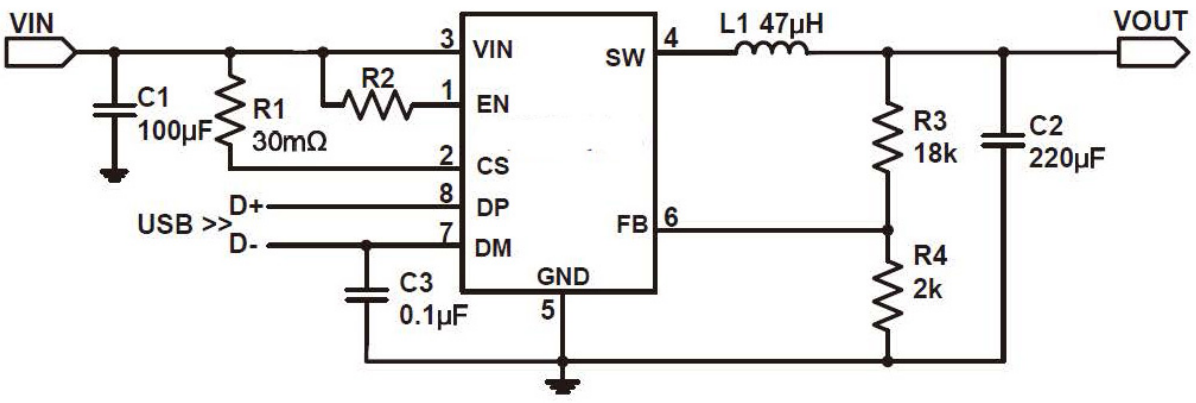
The HM1493 requires a minimum number of readily available standard external components. Other features include cable compensation, UVLO, OVLO, over current protect and thermal shutdown.

The HM1493 converters are available in the industry standard SOP-8L packages.

Application

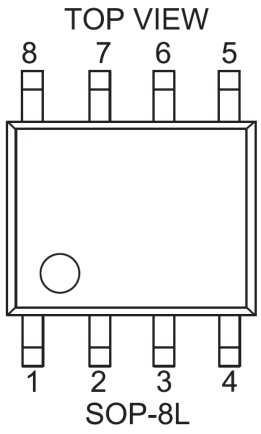
- Car Charger / Adaptor
- Wall-Adapter/ Power Plugs, Outlets
- Mobile/Tablet Power Bank
- USB Power Output Ports

Typical Application Circuit



*The output voltage is set by R3 and R4: V_{OUT} = 0.505V • [1 + (R3/R4)].

Pin Assignment and Description



PIN	NAME	DESCRIPTION
1	EN	ON/OFF Control (High Enable)
2	CS	Current sense
3	VIN	Input Supply Voltage
4	SW	Switch Node
5	GND	Ground
6	FB	Feedback
7	DM	USB DM data line input
8	DP	USB DP data line input

Absolute Maximum Ratings (Note 1)

- Input Supply Voltage .....-0.3V ~ 35V
- SW Voltage .....-0.3V ~ (VIN + 1V)
- DM/DP Pin Voltage.....-0.3V ~ 6V
- Operating Temperature Range (Note 2).....-40℃ ~ +85℃
- Storage Temperature Range..... -65℃ ~ +150℃
- Junction Temperature Range.....+150℃
- Lead Temperature (Soldering, 10 sec.)..... +265℃

Note 1: Stresses beyond those listed Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The HM1493 is guaranteed to meet performance specifications from 0℃ to 70℃. Specifications over the –40℃ to 85℃ operating temperature range are assured by design, characterization and correlation with statistical process controls.

Electrical Characteristics

Operating Conditions: T_A=25℃， V_{IN}=12V,, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Buck DC/DC						
V_{IN}	Operating Voltage Range		10		30	V
I_Q	Quiescent Current	I_{LOAD}=0A	10	15	20	mA
I_{SHDN}	Shutdown Current			110	150	μA
V_{UVLO}	Input UVLO Threshold			4.25	4.5	V
ΔV_{UVLO}	UVLO Hysteresis			50	100	mV
V_{FB}	Regulated Voltage			0.505		V
I_{FB}	Feedback Pin Input Current				0.05	μA
V_{CS}	Current Sense Voltage			80		mV
I_{OUT}	Constant Output Current	R_{CS}=33mΩ，V_{OUT}=4.0V		2.4		A
f_{OSC}	Oscillator Frequency			130		kHz
DC	Max Duty Cycle				100	%
R_{PFET}	$R_{DS(ON)}$ of P-Channel FET			65		mΩ
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET			30		mΩ
T_{SD}	Thermal Shutdown	Temperature Rising		125		℃
ΔT_{SD}	Thermal Shutdown Hysteresis			30		℃
High Voltage Dedicated Charging Port (HXDCP)						
$V_{DAT-REF}$	Date Detect Voltage		0.25	0.325	0.4	V
$T_{GLITCH-DP-H}$	DP High Glitch Filter Time		1000	1250	1500	ms
$T_{GLITCH-DM-L}$	DM Low Glitch Filter Time		1			ms
$T_{GLITCH-V-CHANGE}$	Output Voltage Glitch Filter Time		20	40	60	ms
R_{DM-DWN}	DM Pull-Down Resistance			20		kΩ
DCP 1.2V Charging Mode						
	$DP\_{1.2V}$/$DM\_{1.2V}$ line output voltage		1.08	1.2	1.32	V
	$DP\_{1.2V}$/$DM\_{1.2V}$ line output Impedance			58		kΩ

Pin Functions

EN (Pin 1): ON/OFF Control Pin.

CS (Pin 2): Current Sense Pin. The output current is programmed by connecting resistors, R1: $I_{OUT} = V_{CS}/R1$. (V_{CS} is usually 80mV.)

VIN (Pin 3): Main Supply Pin. The HM1493 operates from 10V to 30V unregulated input. It must be closely decoupled to GND, with a 100μF or greater ceramic capacitor to prevent large voltage spikes from appearing at the input.

SW (Pin 4): Switch Node Connection to the output inductor.

GND (Pin 5): Ground Pin.

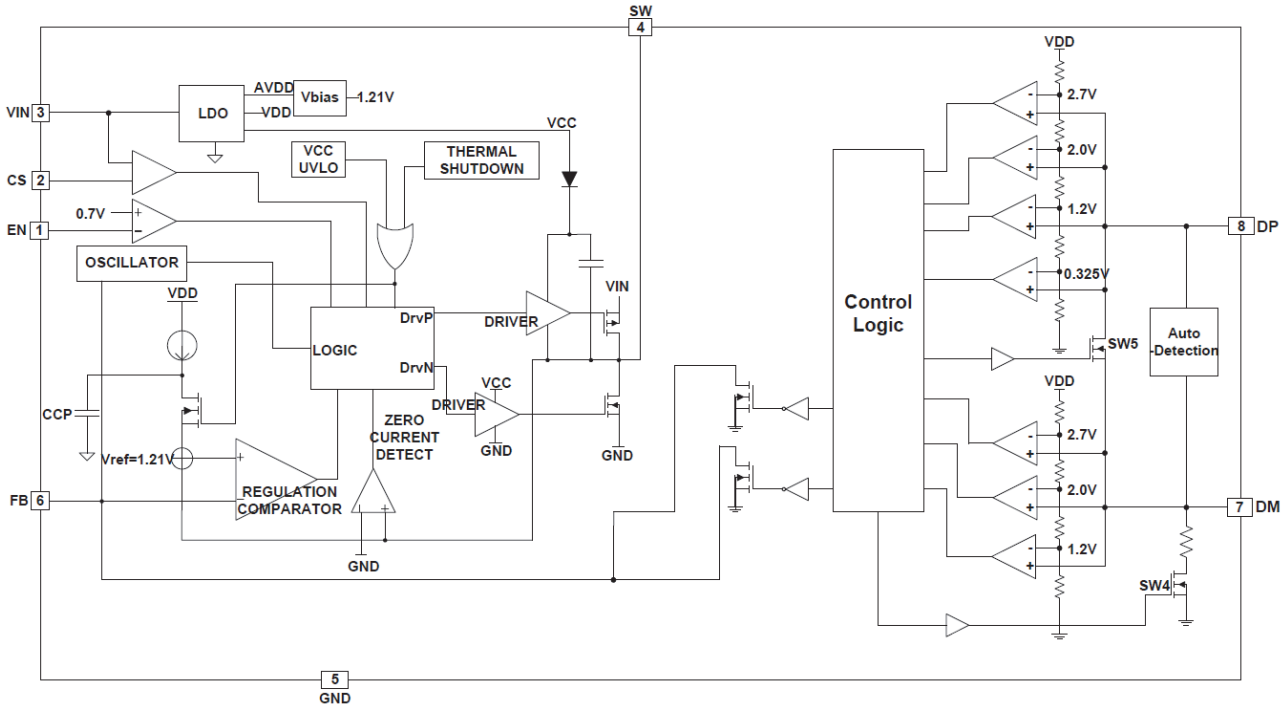
FB (Pin 6): Feedback Pin. Receive the feedback voltage from an external resistive divider across the output. In the adjustable version, the output voltage is fixed. The Output voltage is set by R3 and R4:

$V_{OUT} = 0.505V \bullet [1 + (R3/R4)]$.

DM (Pin 7): USB DM data line input.

DP (Pin 8): USB DP data line input.

Block Diagram



Application Information

Quick Charge 2.0 High Voltage Dedicated Charging Port (HVDCP) Specifications

The HVDCP specification details a simple method for a downstream device to request a higher voltage from the upstream AC/DC adapter while maintaining USB battery Charging 1.2 compatibility and allowing compatibility with other specifications that use the USB ID pin or communicate on USB VBUS. There is Class A of HVDCP upstream devices, class A must be capable of outputting 5V at the beginning, and then 9V or 12V. These voltages are based on the capabilities of the downstream device. The downstream device will request an output voltage for the HVDCP.

Quick Charge 2.0 Interface

The HM1493 supports the full output voltage range of Quick Charge 2.0 Class A (5V, 9V, or 12V. It automatically detects either Quick Charge 2.0 capable powered devices (PD) or legacy PDs compliant with the USB Battery Charging Specification 1.2 and only enables output voltage adjustment accordingly.

The HM1493 with DP and DM short-circuited the normal handshake between the AC/DC adapter and powered devices (PD) as described in the USB Battery Charging Specification 1.2 can commence. After HM1493 starts monitoring the voltage level at DP. If DP continuously stays above 0.325 V for at least 1.25 seconds and will enter Quick Charge 2.0 operation mode. If voltage at DP drops any time below 0.325V resets 1.25 seconds timer and stays in USB Battery Charging Specification 1.2 compatibility mode with a default output voltage of 5V.

Once HM1493 has entered Quick Charge 2.0 operation mode, a 19.53kΩ pull-down resistor is connected to DM. As soon as the voltage at DM has dropped low (<0.325V) for at least 1 ms starts accepting requests for different AC-DC adapter output voltages by means of applied voltage levels at data lines DP and DM through the powered device.

Table1: HVDCP Voltage and Status

DP	DM	VOUT(V)
0.6	0.6	12
3.3	0.6	9
0.6	GND	5

Thermal Protection

The total power dissipation in HM1493 is limited by a thermal protection circuit. When the device temperature rises to approximately 125℃, this circuit turns off the output, allowing the IC to cool. The thermal protection circuit can protect the device from being damaged by overheating in the event of fault conditions. Continuously running the HM1493 into thermal shutdown degrades device reliability.

Current Limit

Current limit detection occurs during the off-time by monitoring the current through the low-side switch using an external resistor, R_{CS}. The current limit value is defined by R_{CS}. If during the off-time the current in the low-side switch exceeds the user defined current limit value, the next on-time cycle is immediately terminated. Current sensing is achieved by comparing the voltage across the low side FET with the voltage across the current limit set resistor R_{CS}. For example, the current limit value is 2.4A by the R_{CS} =33mΩ. The current limit value rises when the set resistor R_{CS} rises. The maximum output current is set by R_{CS}: R_{CS} (kΩ) = V_{CS}/I_{MAX} (A).

Setting Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. It is recommended to use divider resistors with 1% tolerance or better. To improve efficiency at very light loads consider using larger value resistors. If the values are too high the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable. For most applications, a resistor in the 10kΩ to 1MΩ range is suggested for R4. R3 is then given by:

$$R3 = R4 \bullet [(V_{OUT} / V_{REF}) – 1]$$

where V_{REF} is 0.505V.

Inductor Selection

For most applications, the value of the inductor will fall in the range of 4.7μH to 47μH. Its value is chosen based on the desired ripple current. Large value inductors lower ripple current and small value inductors result in higher ripple currents. Higher V_{IN} or V_{OUT} also increases the ripple current and value inductors result in higher ripple currents.

Higher V_{IN} or V_{OUT} also increases the ripple current as shown in equation. A reasonable starting point for setting ripple current is ΔI_L=1000mA (40% of 2.5A).

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 3.5A rated inductor should be enough for most applications (2.5A + 1000mA). For better efficiency, choose a low DC-resistance inductor.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or perm alloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs. size requirements and any radiated field/EMI requirements than on what the HM1493 requires to operate.

Output and Input Capacitor Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{required}\ I_{RMS} \cong I_{OMAX} \frac{\left[V_{OUT}(V_{IN} - V_{OUT})\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the IRIPPLE(P-P) requirement. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta I_L\left(ESR + \frac{1}{8fC_{OUT}}\right)$$

Where f = operating frequency, C_{OUT} = output capacitance and ΔIL = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔIL increases with input voltage.

Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum. These are specially constructed and tested for low ESR so they give the lowest ESR for a given volume.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as: Efficiency = 100% - (L1+ L2+ L3+ ...) where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: V_{IN} quiescent current and I^2R losses. The V_{IN} quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The V_{IN} quiescent current is due to two components: the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge ΔQ moves from VIN to ground. The resulting ΔQ/Δt is the current out of VIN that is typically larger than the DC bias current.

In continuous mode, $I_{GATECHG} = f(Q_T+Q_B)$ where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to VIN and thus

their effects will be more pronounced at higher supply voltages.

2. I^2R losses are calculated from the resistances of the internal switches, R_{SW} and external inductor R_L. In continuous mode the average output current flowing through inductor L is “chopped” between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows: $R_{SW} = R_{DS(ON)TOP} \times DC + R_{DS(ON)BOT} \times (1-DC)$ The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current. Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

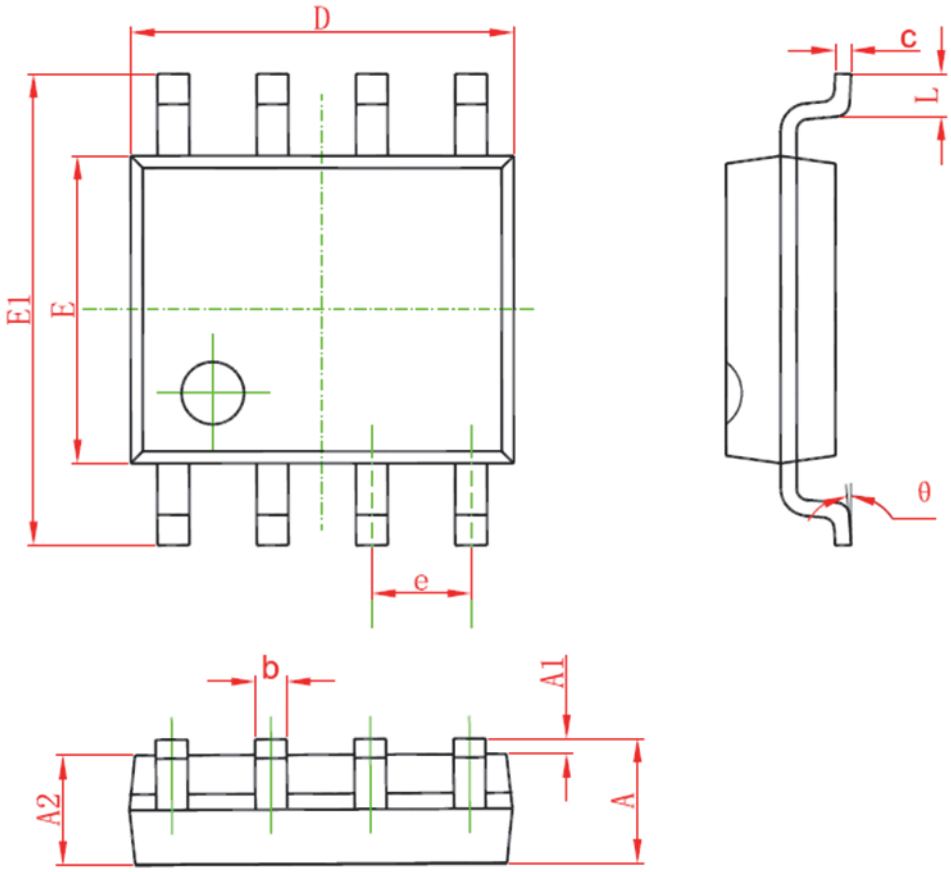
Board Layout Suggestions

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the HM1493. Check the following in your layout.

1. The power traces, consisting of the GND trace, the SW trace and the VIN trace should be kept short, direct and wide.
2. Put the input capacitor as close as possible to the device pins (V_{IN} and GND).
3. SW node is with high frequency voltage swing and should be kept small area. Keep analog components away from SW node to prevent stray capacitive noise pick-up.
4. Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacitors.

Packaging Information

SOP-8L Package Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°