# HM1542

## Tiny Package, High Efficiency, Step-up DC/DC Converter

## Features

- Output up to 24V
- Internal MOSFET with high switch current up to 3A
- 19μA Quiescent (Switch-off) Supply Current
- Zero Shutdown Mode Supply Current
- 90% Efficiency
- Up to 450KHz Switching Frequency
- Using Internal Power Switches
- SOT-23-6 Package

## Applications

- PDA
- DSC
- LCD Panel
- RF-Tags
- MP3
- Portable Instrument
- Wireless Equipment

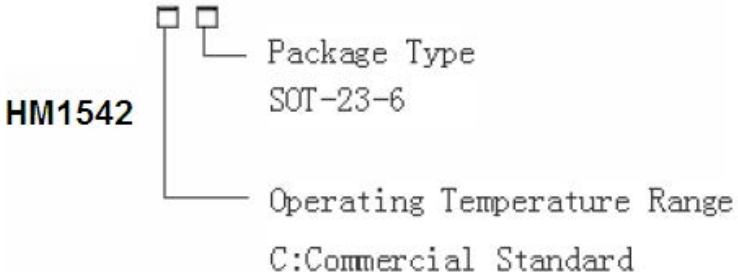
## Description

The HM1542 is a compact, high efficiency, and low voltage step-up DC/DC converter including an error amplifier, ramp generator, comparator, switch pass element and driver in which providing a stable and high efficient operation over a wide range of load currents. It operates in stable waveforms without external compensation.

The low start-up input voltage below 1.6V. The high switching rate minimized the size of external components. Besides, the 19μA low quiescent current together with high efficiency maintains long battery lifetime.

The output voltage is set with two external resistors.

## Ordering Information



## Typical Application

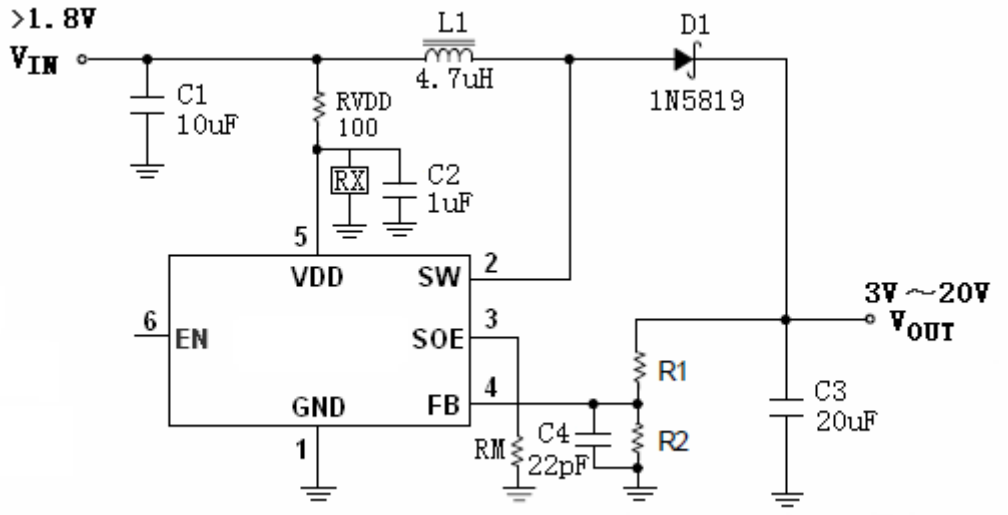



Figure 1 (1.8V Stat-up input Voltage)

RX can be a Zener Diodes or Resistor: The Ratio of RX/RVDD must to keep VDD voltage less than 5.5V.

＊ The resistor RM can be set to 50mΩ usually.

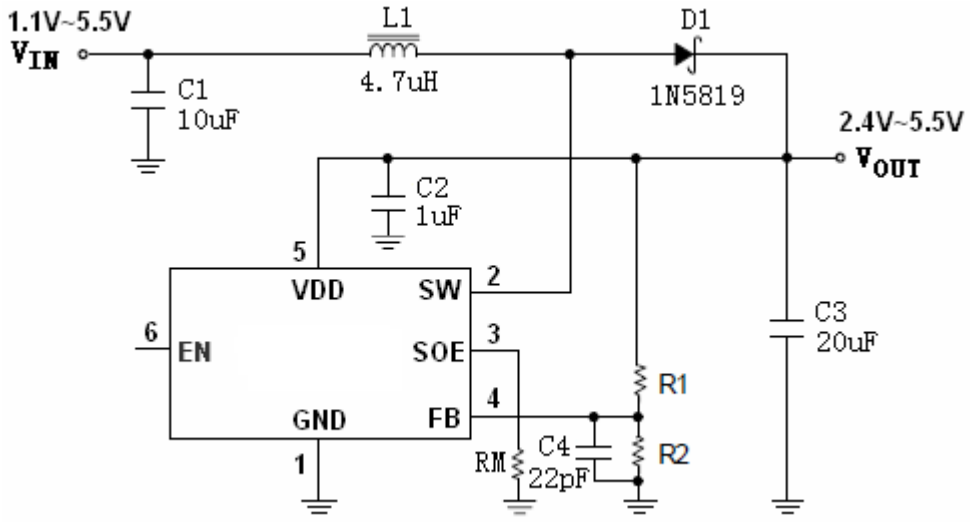



Figure.2 （1.1V Stat-up input Voltage）

＊ The resistor RM can be set to 50mΩ usually

## Test Circuit

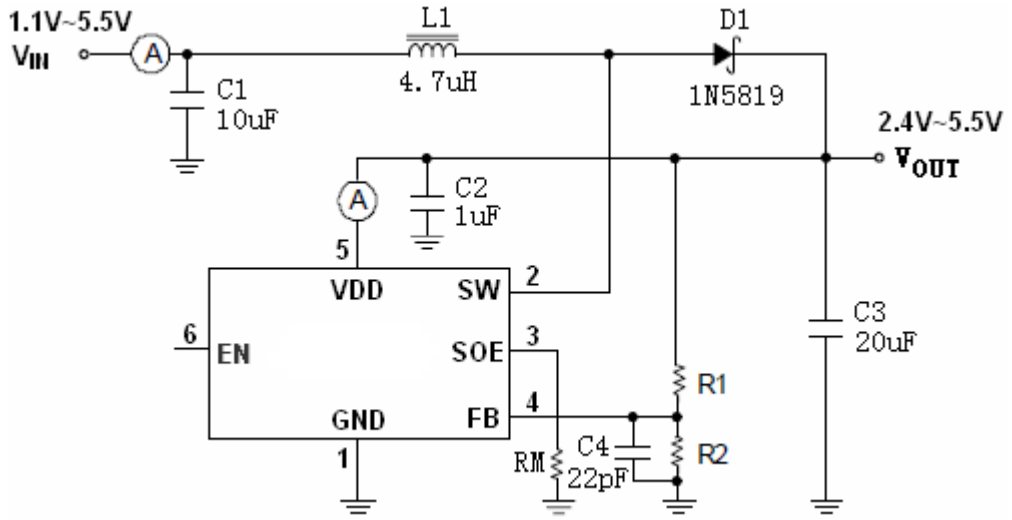



Figure 3

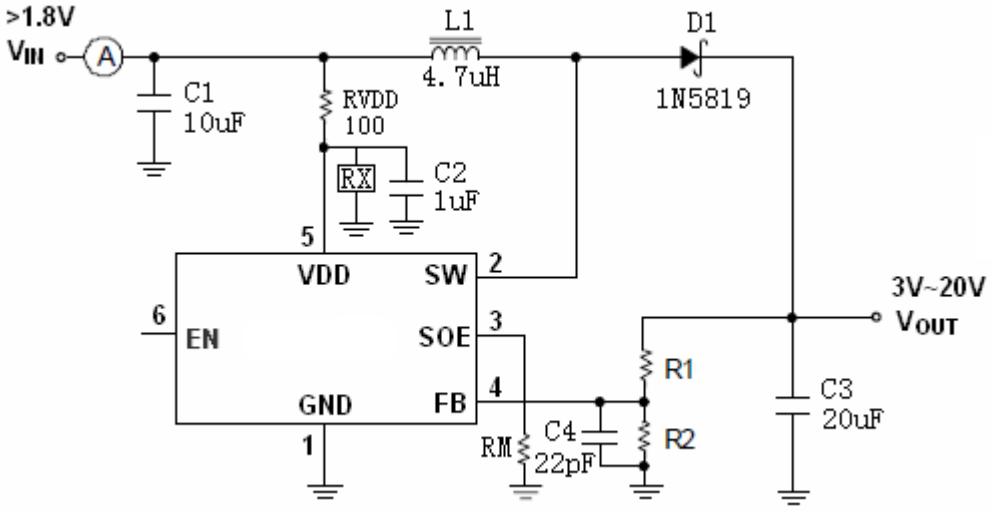
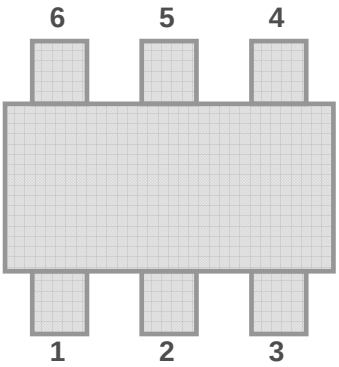



Figure 4

## Absolute Maximum Ratings

- Supply Voltage……-0.3V to 6V
- SW Pin Switch Voltage……-0.3V to 28V
- Other I/O Pin Voltages……-0.3V to 6V
- SW Pin Switch Current ……3A
- Operating Junction Temperature……125℃
- Storage Temperature Range ……-65℃ ~ +150℃

## Pin Assignment




| PIN NUMBER SOT-23-6 | PIN NAME | FUNCTION |
|---|---|---|
| 1 | GND | Ground |
| 2 | SW | Switch Output |
| 3 | SOE | Source of the MOSFET |
| 4 | FB | Feedback |
| 5 | VDD | Output |
| 6 | EN | ON/OFF Control(High Enable) |

## Electrical Characteristics

($V_{IN}$ = 1.5V, VDD set to 3.3V, Load Current = 0A, TA = 25℃, unless otherwise specified)

| Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Start-UP Voltage | IL = 1mA | 1.00 | | | V |
| Operating VDD Range | VDD pin voltage | 2 | | 5.5 | V |
| No Load Current I ($V_{IN}$) | $V_{IN}$ = 1.5V, $V_{OUT}$ = 3.3V | | 40 | | μA |
| Feedback Reference Voltage | Close Loop, VDD = 3.3V | 1.182 | 1.212 | 1.242 | V |
| Switching Frequency | VDD = 3.3V | | | 450 | KHz |
| Maximum Duty | VDD = 3.3V | | 80 | | % |
| SW ON Resistance | VDD = 3.3V | | 0.07 | | Ω |
| Current Limit Setting | VDD = 3.3V | | 3 | | A |
| Line Regulation | $V_{IN}$ = 1.5 ~ 2.5V, IL = 100mA | | 55 | | mV/V |
| Load Regulation | $V_{IN}$ = 2.5V, IL = 1 ~ 300mA | | 0.1 | | mV/mA |
| En Input High | | 1 | | | V |
| En Input Low | | | | 0.6 | V |
| Temperature Stability for $V_{OUT}$ | | | 50 | | ppm/℃ |
| Thermal Shutdown | | | 165 | | ℃ |
| Thermal Shutdown Hysterics | | | 10 | | ℃ |
| Maximum $V_{RM}$ | | | 145 | | mV |

## Test Circuit

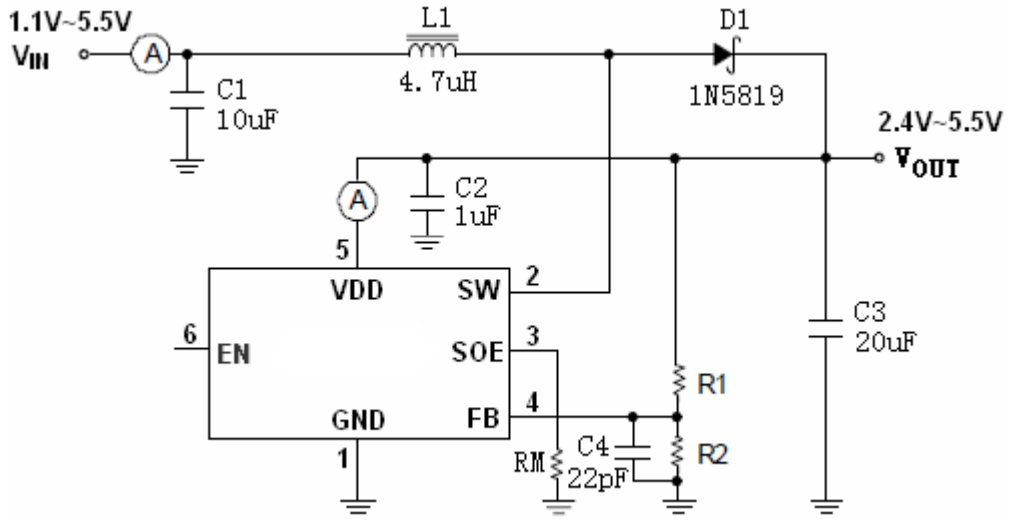



Figure 3

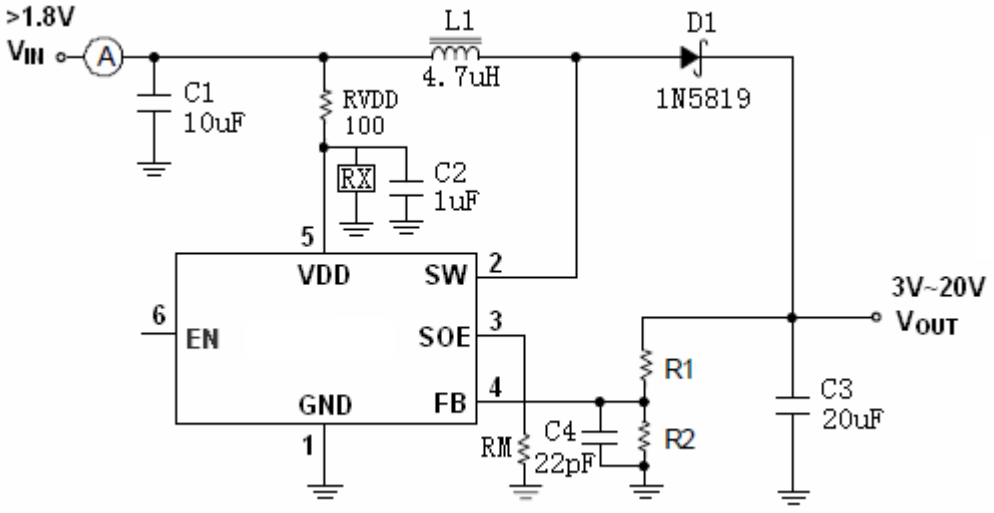



Figure 4

## Absolute Maximum Ratings

- Supply Voltage……-0.3V to 6V
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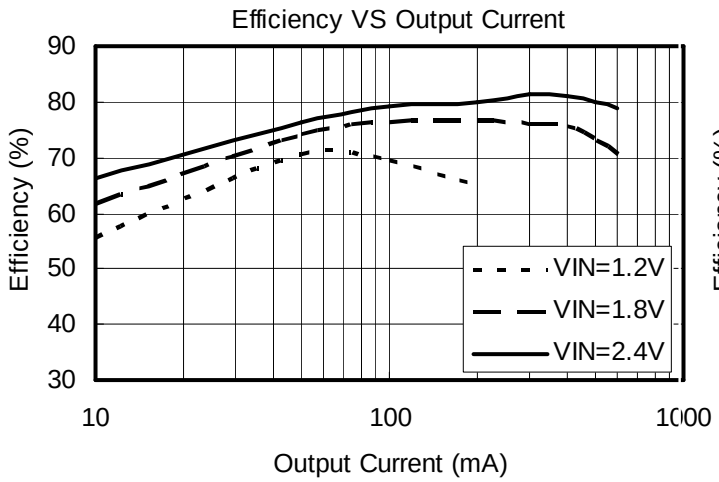
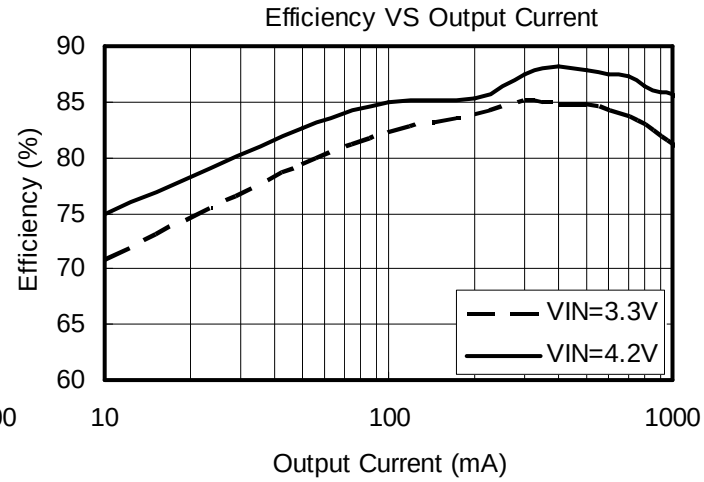
- Other I/O Pin Voltages……-0.3V to 6V
- SW Pin Switch Current ……3A
- Operating Junction Temperature……125℃
- Storage Temperature Range ……-65℃ ~ +150℃

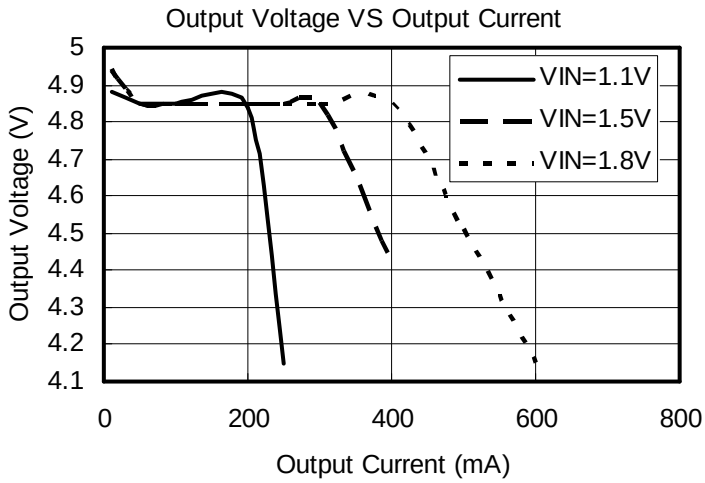
## Typical Performance Characteristics

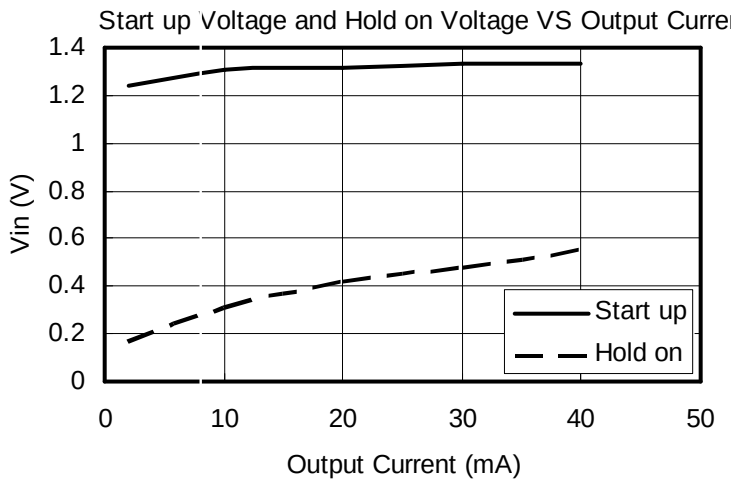
TA=25℃, $C_{IN}$ =10 μF, $C_{OUT}$ =20 μF, L=4.7 μH, unless otherwise noted.

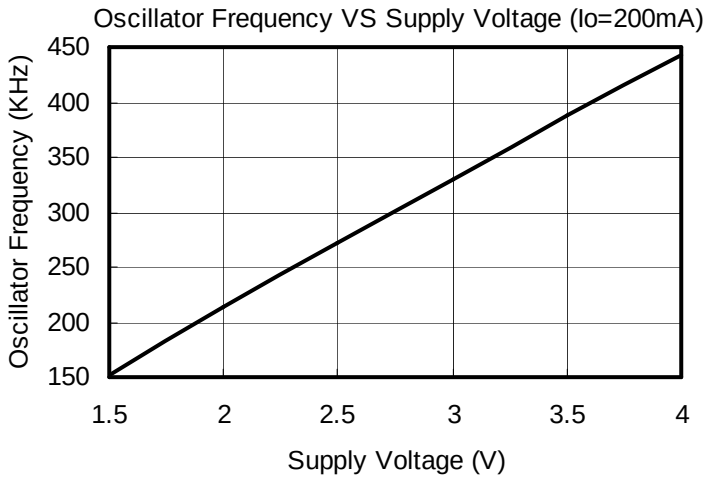
VOUT=5V (RM=0.33/5Ω)



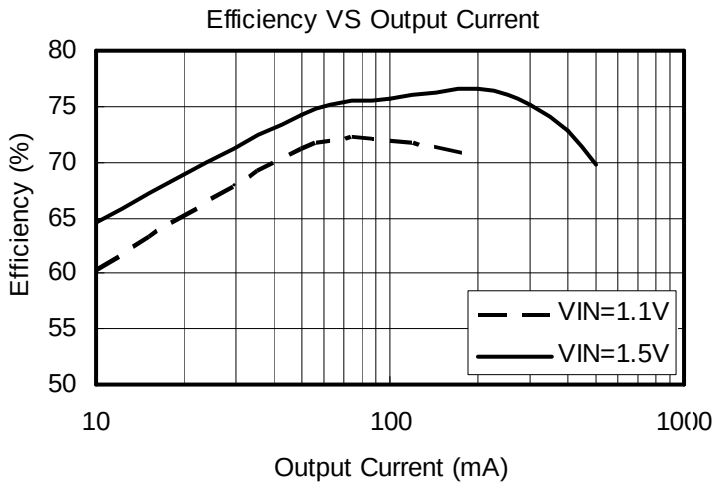



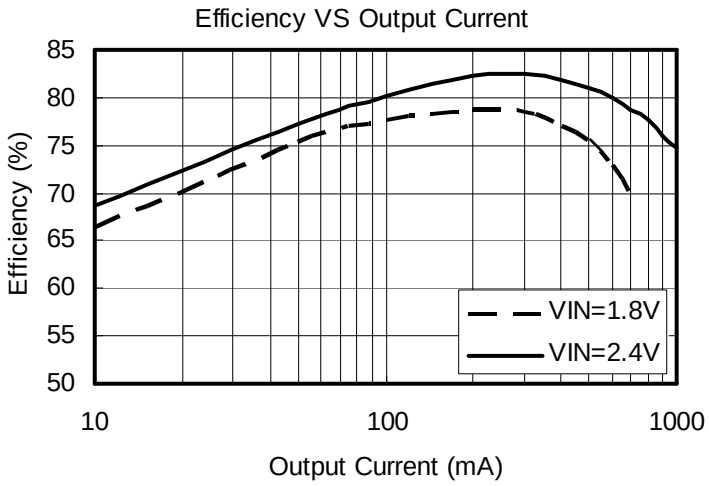



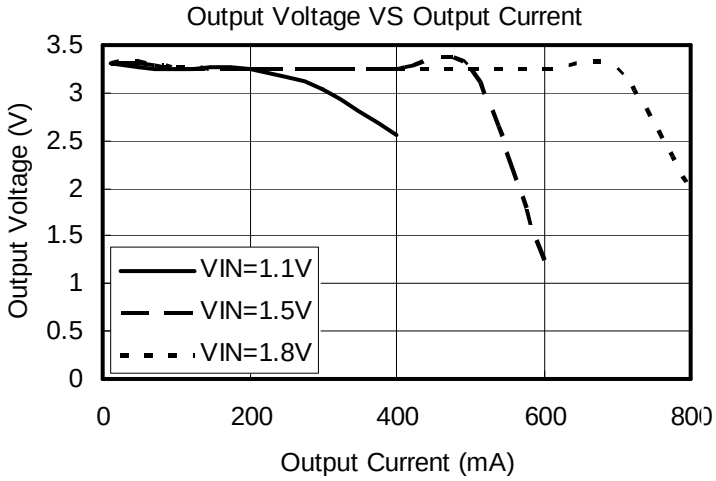
## Typical Performance Characteristics

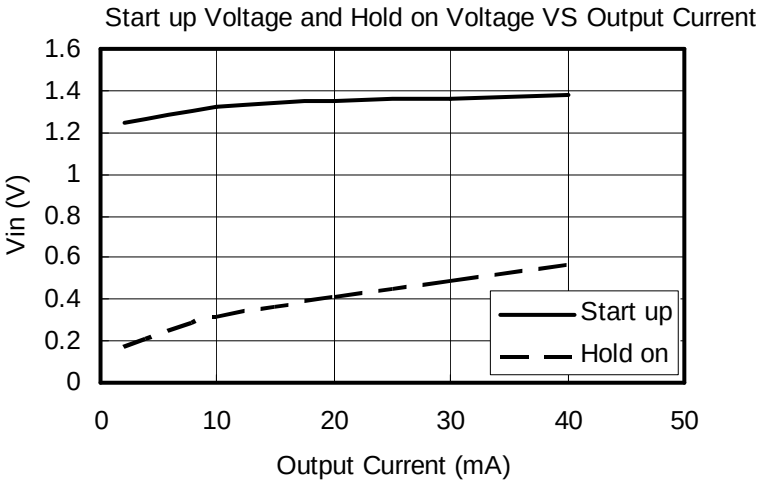
TA=25℃, $C_{IN}$ =10 μF, $C_{OUT}$ =20 μF, L=4.7 μH, unless otherwise noted.
Refer to Test Circuit Figure. 1

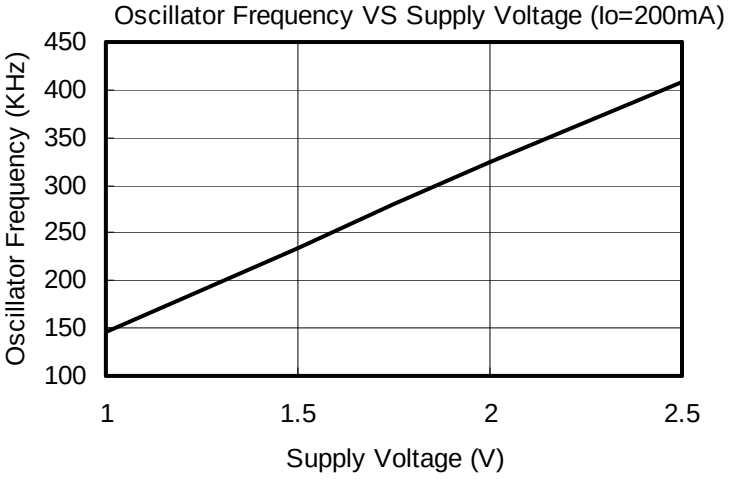
VOUT=3.3V (RM=0.33/5 Ω)



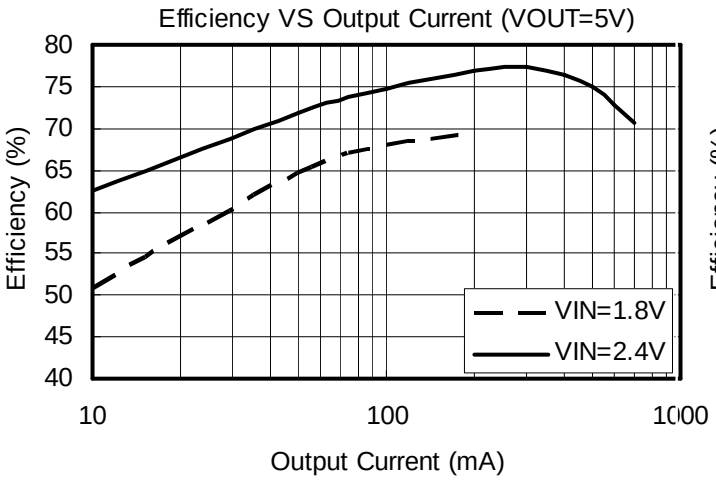



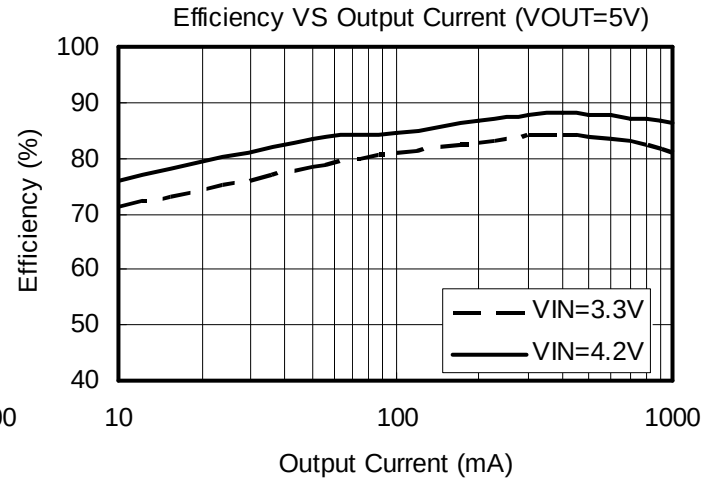



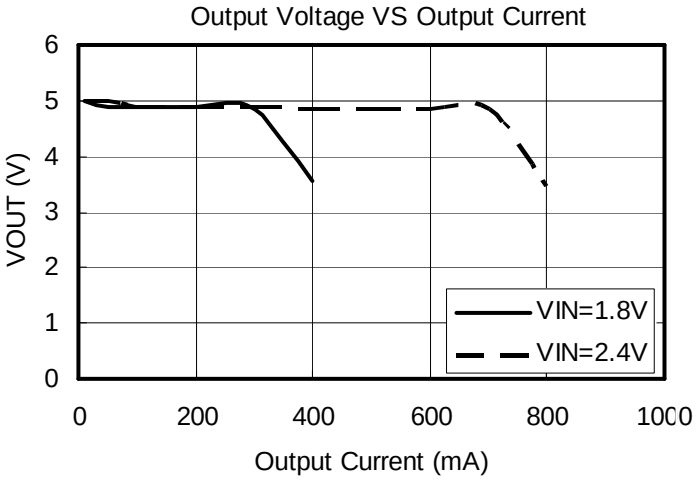
## Typical Performance Characteristics

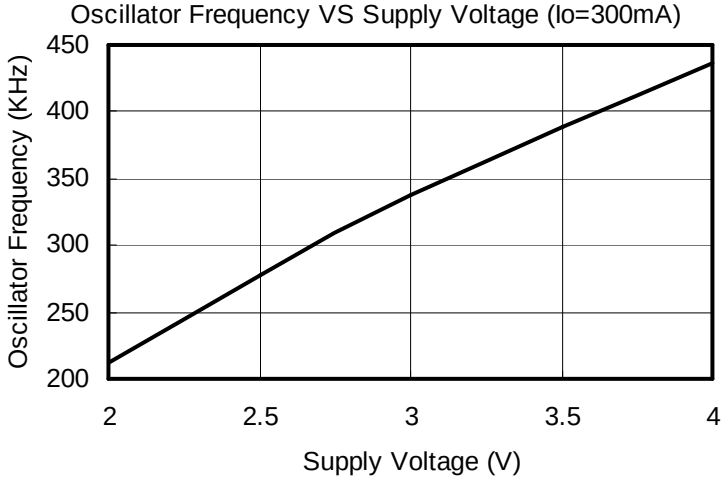
$T_A$=25℃, $C_{IN}$ =10 μF, $C_{OUT}$ =20 μF, L=4.7 μH, unless otherwise noted.
Refer to Test Circuit Figure. 2

$V_{OUT}$=5V (RM=0.33/5Ω)



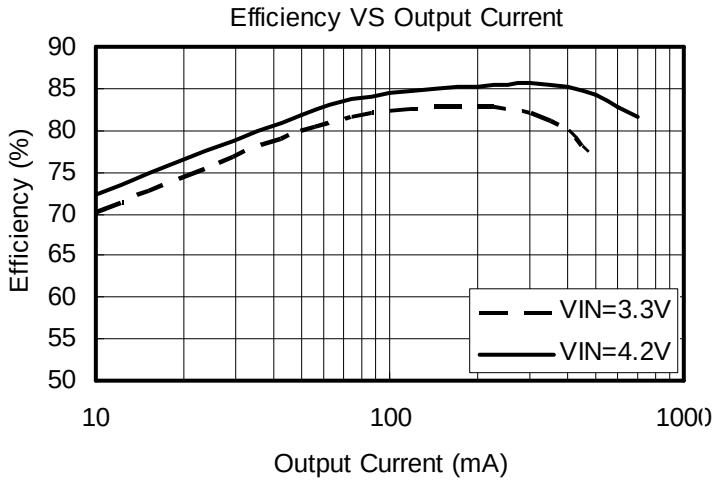



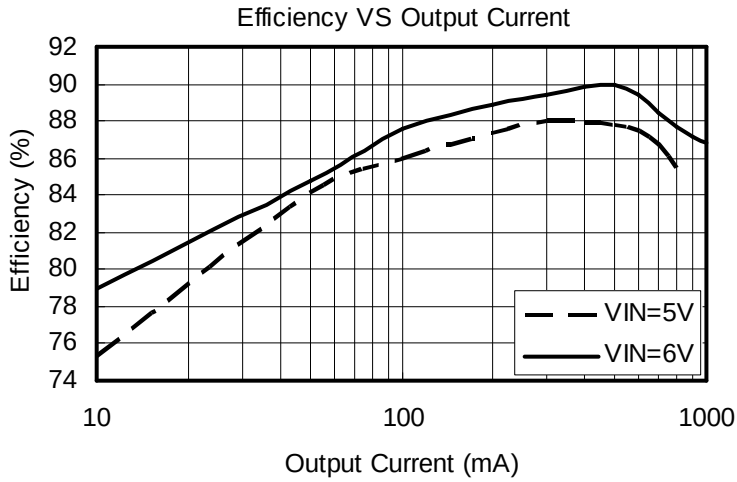



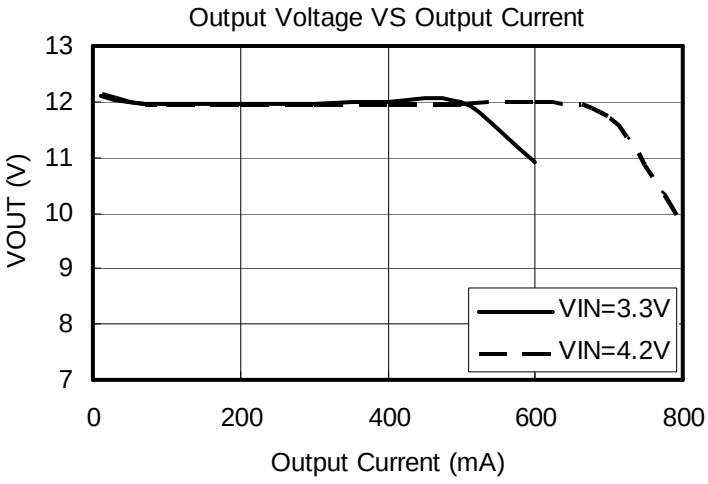
## Typical Performance Characteristics

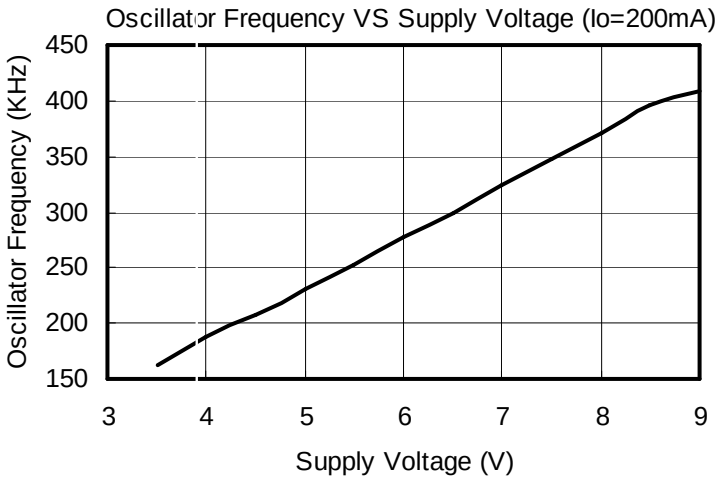
$T_A$=25℃, $C_{IN}$ =10 μF, $C_{OUT}$ =20 μF, L=10 μH (high saturated inductor current), unless otherwise noted.

$V_{OUT}$=12V (RM=0.33/7Ω)

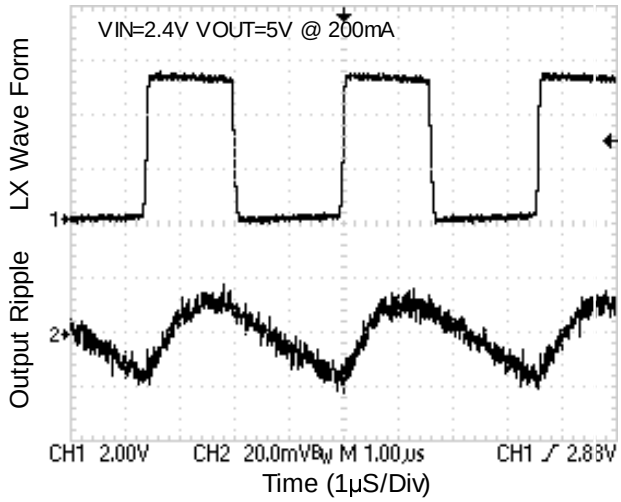


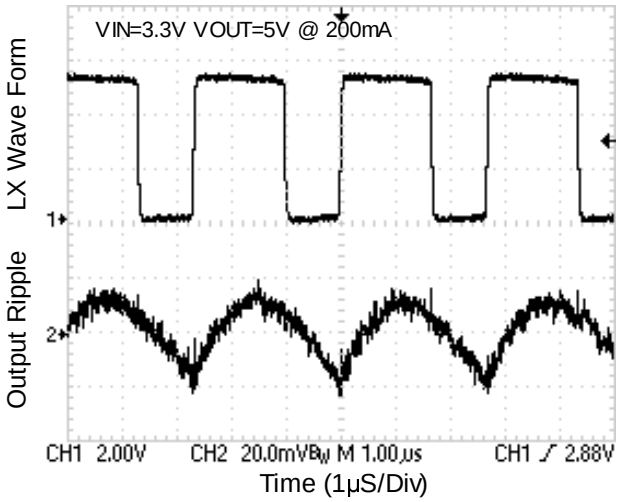



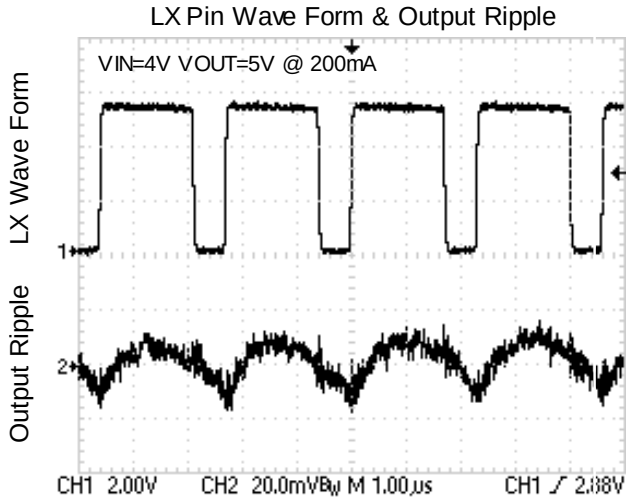
LX Pin Wave Form & Output Ripple



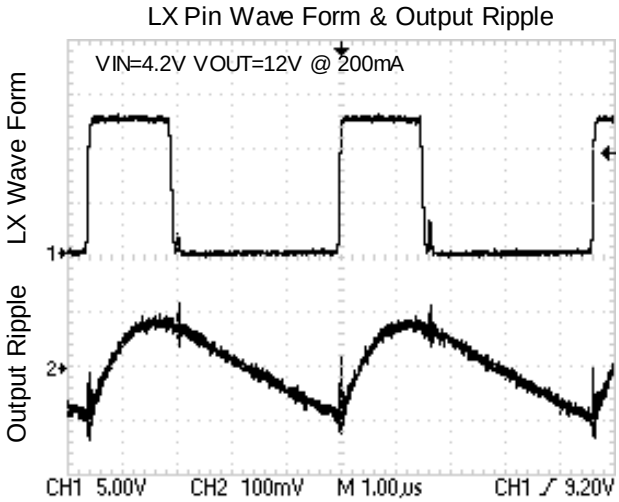

LX Pin Wave Form & Output Ripple



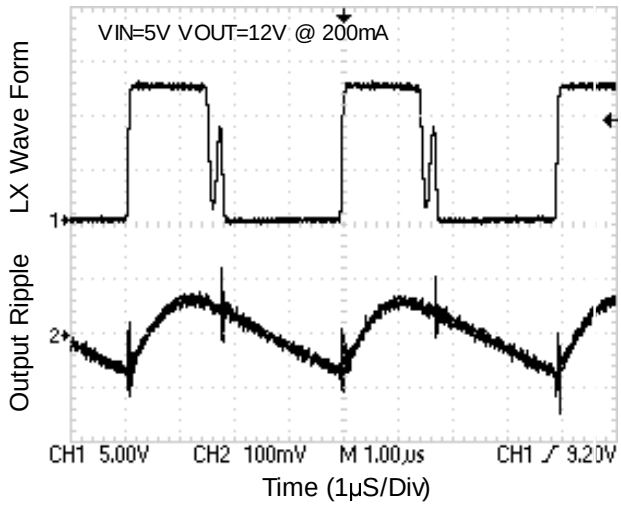

LX Pin Wave Form & Output Ripple



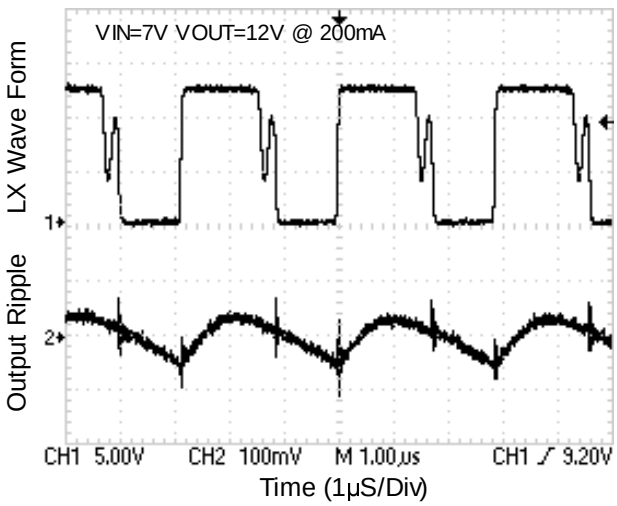

LX Pin Wave Form & Output Ripple




LX Pin Wave Form & Output Ripple




LX Pin Wave Form & Output Ripple



## Pin Information

GND (Pin 1): Signal and Power Ground. Provide a short direct PCB path between GND and the (–) side of the output capacitor(s).

SW (Pin 2): Switch Pin. Connect inductor between SW and $V_{IN}$. Keep these PCB trace lengths as short and wide as possible to reduce EMI and voltage overshoot.

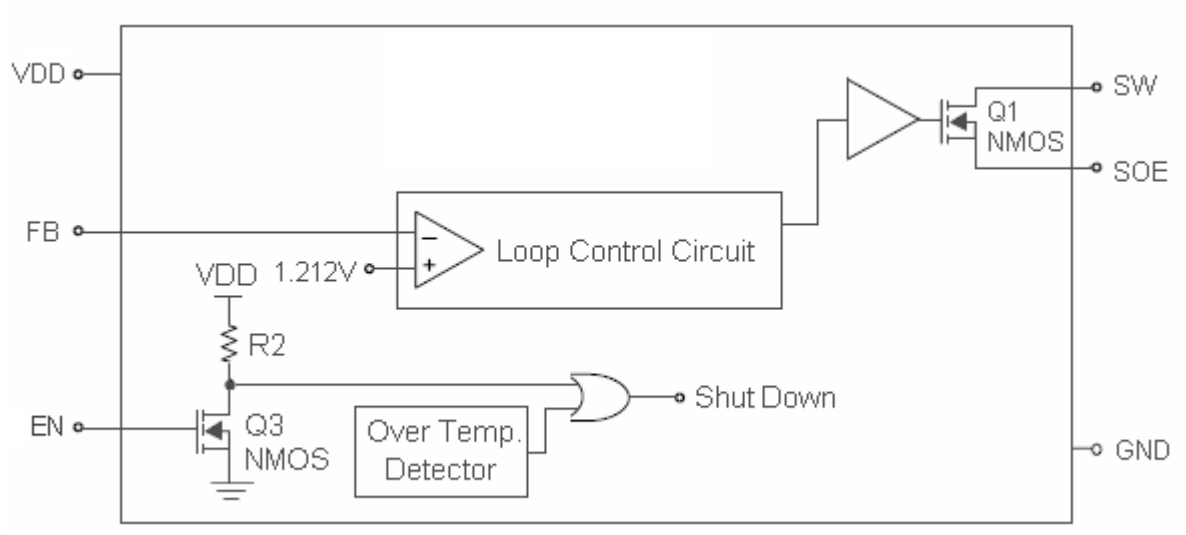
SOE (Pin 3): Source of the MOSFET. Connect resistor to GND

FB (Pin 4): Feedback Input to the $g_m$ Error Amplifier. Connect resistor divider tap to this pin. The output voltage can be adjusted from 3.3V to 20V by: $V_{OUT} = 1.212V \bullet [1 + (R1/R2)]$

VDD (Pin 5): Input positive power pin.

EN (Pin 6): En Control Input. Forcing this pin above 1V enables the part. Forcing this pin below 0.6V shuts down the device. In shutdown, all functions are disabled, drawing <1μA supply current. Do not leave EN floating.

## Functional Diagram



## Application Information

### Output Voltage Setting

Referring to Typical Application Circuits, the output voltage of the switching regulator ($V_{OUT}$) can be set with Equation (1).

$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) \times 1.212\ V \quad (1)$$

### Current-limiting Resistance Setting

$$RM = \frac{0.145}{I_{MAX\text{-}switch}}$$

### Feedback Loop Design

Referring to the typical application circuits, the selection of R1 and R2 based on the trade-off between quiescent current consumption and interference immunity is stated below:

For applications without standby or suspend modes, lower values of R1 and R2 are preferred. For applications concerning the current consumption in standby or suspend modes, the higher values of R1 and R2 are needed. Such high impedance feedback loop is sensitive to any interference, which requires careful PCB layout and avoid any interference, especially to FB pin. To improve the system stability, a proper value capacitor between FB pin and GND pin is suggested. An empirical suggestion is around 20pF.

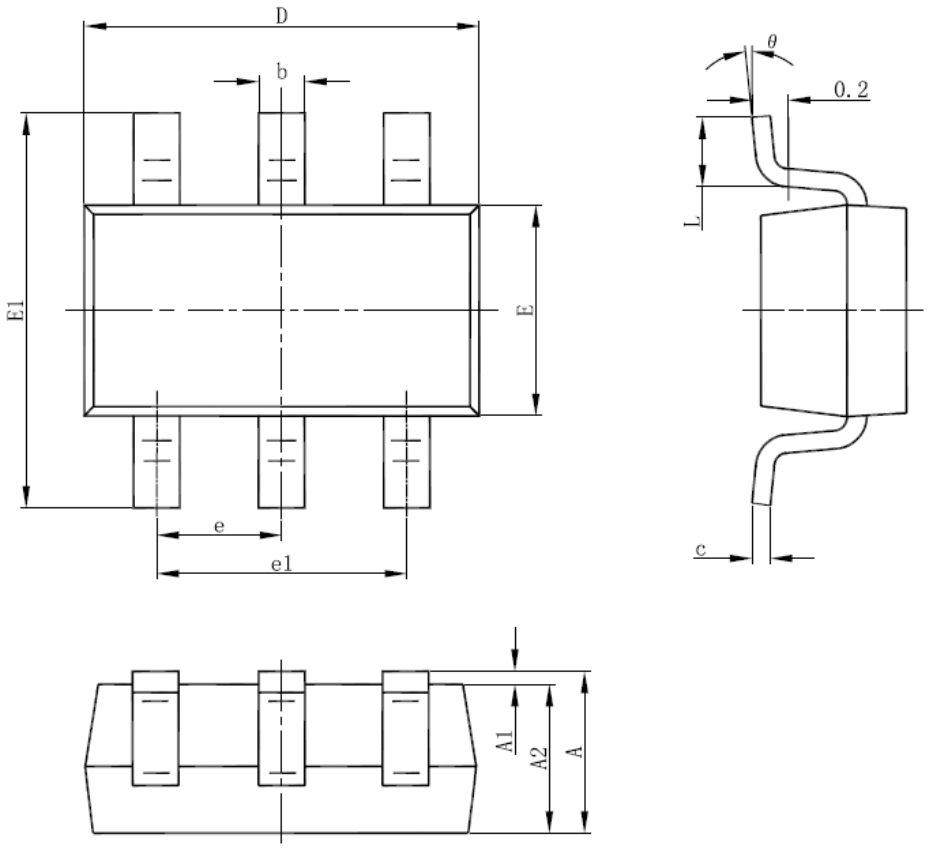
### PCB Layout Guide

PCB Layout shall follow these guidelines for better system stability:

- A full GND plane without any gap break.
- VDD to GND bypass Cap – The 1μF MLCC noise bypass Cap pin 4 shall have short and wide connections.
- $V_{IN}$ to GND bypass Cap – Add a Cap close to the inductor when $V_{IN}$ is not an idea voltage source.
- Minimize the FB node copper area and keep it far away from noise sources.
- l Follow Equation (1)
- l Higher R reduces the quiescent current (Path current = 1.212V/R2), however resistors beyond 5MW are not Recommended.

## Packaging Information

SOT-23-6 Package Outline Dimension




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.050 | 1.250 | 0.041 | 0.049 |
| A1 | 0.000 | 0.100 | 0.000 | 0.004 |
| A2 | 1.050 | 1.150 | 0.041 | 0.045 |
| b | 0.300 | 0.500 | 0.012 | 0.020 |
| c | 0.100 | 0.200 | 0.004 | 0.008 |
| D | 2.820 | 3.020 | 0.111 | 0.119 |
| E | 1.500 | 1.700 | 0.059 | 0.067 |
| E1 | 2.650 | 2.950 | 0.104 | 0.116 |
| e | 0.950(BSC) | | 0.037(BSC) | |
| e1 | 1.800 | 2.000 | 0.071 | 0.079 |
| L | 0.300 | 0.600 | 0.012 | 0.024 |
| | 0° | 8° | 0° | 8° |