

## P-Channel Enhancement Mode Power MOSFET

### **Description**

The PT FÍ ÚF€Ö uses advanced trench technology and design to provide excellent R<sub>DS(ON)</sub> with low gate charge. It can be used in a wide variety of applications. It is ESD protested.

#### **General Features**

V<sub>DS</sub> =-100V,I<sub>D</sub> =-FÍ A

 $R_{DS(ON)}$  <58m $\Omega$  @  $V_{GS}$ =-10V (Typ:44m $\Omega$ )

 $R_{DS(ON)}$  <65m $\Omega$  @  $V_{GS}$ =--4.5V (Typ:48m $\Omega$ )

- Super high dense cell design
- Advanced trench process technology
- Reliable and rugged
- High density cell design for ultra low On-Resistance

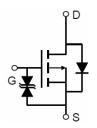
### **Application**

Portable equipment and battery powered systems

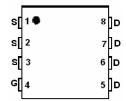
100% ΔVds TESTED!

100% UIS TESTED!

.....



Schematic diagram



"Märking and pin assignment

**Package Marking and Ordering Information** 

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
ÁRT FÍ ÚF€Ö	ÁAPT FÍ ÚF€Ö	ÁKÖØÞÍÝÎËÌŠ			-

Absolute Maximum Ratings (T<sub>C</sub>=25 ℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	-100	V
Gate-Source Voltage	V <sub>G</sub> s	±20	V
Drain Current-Continuous	I <sub>D</sub>	-FÍ	А
Drain Current-Continuous(T <sub>C</sub> =100°C)	I <sub>D</sub> (100℃)	-F€	Α
Pulsed Drain Current	I <sub>DM</sub>	ÁI Í	Α
Maximum Power Dissipation	P <sub>D</sub>	120	W
Derating factor		0.8	W/°C
Operating Junction and Storage Temperature Range	$T_{J}$ , $T_{STG}$	-55 To 175	$^{\circ}$

#### **Thermal Characteristic**

Thermal Resistance, Junction-to-Case (Note 2)	R <sub>θJc</sub>	1.25	°C/W
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# Electrical Characteristics (T<sub>C</sub>=25 °C unless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =-250μA	-100	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-100V,V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V,V <sub>DS</sub> =0V	-	-	±10	μA
On Characteristics (Note 3)	·		•			
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ , $I_{D}=-250\mu A$	-1.5	-1.9	-2.5	V
Drain-Source On-State Resistance	В	V <sub>GS</sub> =-10V, I <sub>D</sub> =-15A	-	44	58	mΩ
Diam-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-15A	-	48	65	mΩ
Forward Transconductance	<b>g</b> FS	V <sub>DS</sub> =-50V,I <sub>D</sub> =-10A	5	-	-	S
Dynamic Characteristics (Note4)	·		•			
Input Capacitance	C <sub>lss</sub>	V <sub>DS</sub> =-50V,V <sub>GS</sub> =0V,	-	3810	-	PF
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> =-50V,V <sub>GS</sub> =0V, F=1.0MHz	-	93	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>	F=1.0WHZ	-	91	-	PF
Switching Characteristics (Note 4)	·		•			
Turn-on Delay Time	t <sub>d(on)</sub>		-	17	-	nS
Turn-on Rise Time	t <sub>r</sub>	V <sub>DD</sub> =-50V,I <sub>D</sub> =-15A	-	80	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>	$V_{GS}$ =-10V, $R_{GEN}$ =9.1 $\Omega$	-	45	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	65	-	nS
Total Gate Charge	Qg	\/ - 50\/   - 45^	-	136	-	nC
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS}$ =-50V, $I_{D}$ =-15A, $V_{GS}$ =-10V	-	22	-	nC
Gate-Drain Charge	$Q_{gd}$	V <sub>GS</sub> 10V	-	26	-	nC
Drain-Source Diode Characteristics	·		•			
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V,I <sub>S</sub> =-10A	-	-	-1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>	-	-	-	-FÍ	Α
Reverse Recovery Time	t <sub>rr</sub>	TJ = 25°C, IF =-15A	-	90	-	nS
Reverse Recovery Charge	Qrr	di/dt = 100A/µs <sup>(Note3)</sup>	-	70	-	nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negli	gible (turr	n-on is do	minated b	y LS+LD)

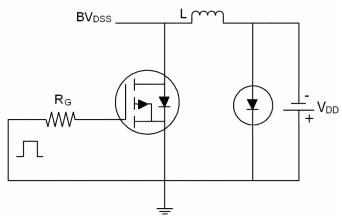
## Notes:

- $\textbf{1.} \ \textbf{Repetitive Rating: Pulse width limited by maximum junction temperature.}$
- **2.** Surface Mounted on FR4 Board,  $t \le 10$  sec.
- 3. Pulse Test: Pulse Width  $\leq$  300 $\mu$ s, Duty Cycle  $\leq$  2%.
- 4. Guaranteed by design, not subject to production

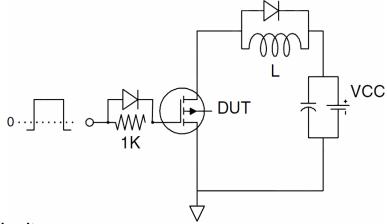


## **Test Circuit**

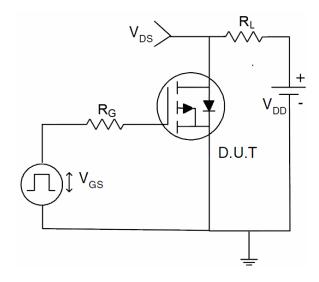
# 1) E<sub>AS</sub> Test Circuit



# 2) Gate Charge Test Circuit

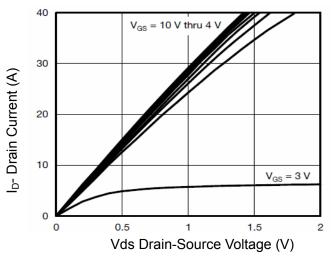


## 3) Switch Time Test Circuit

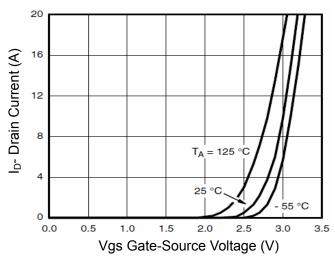




## **Typical Electrical and Thermal Characteristics (Curves)**



**Figure 1 Output Characteristics** 



**Figure 2 Transfer Characteristics** 

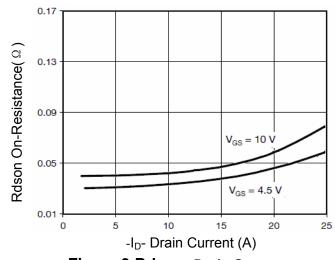


Figure 3 Rdson- Drain Current

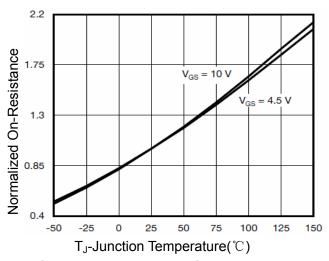


Figure 4 Rdson-JunctionTemperature

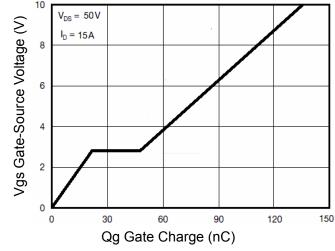


Figure 5 Gate Charge

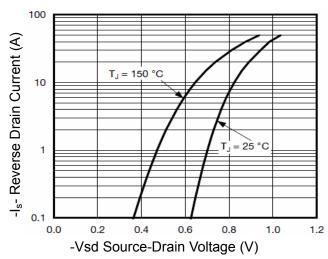


Figure 6 Source- Drain Diode Forward



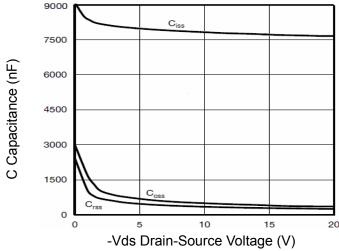
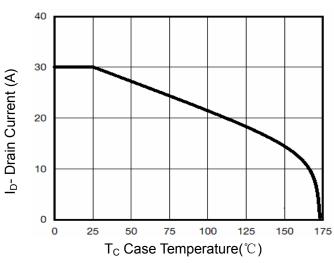
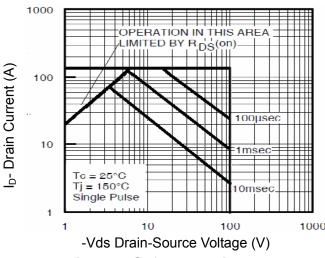


Figure 7 Capacitance vs Vds



**Figure 9 Drain Current vs Case Temperature** 



**Figure 8 Safe Operation Area** 

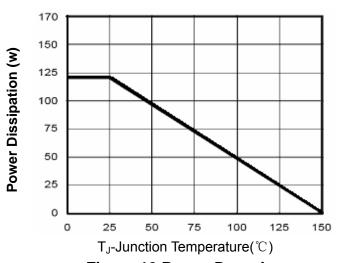
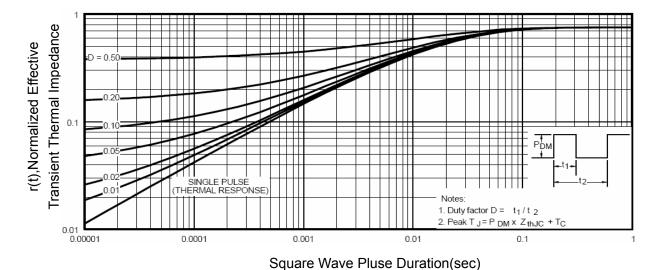


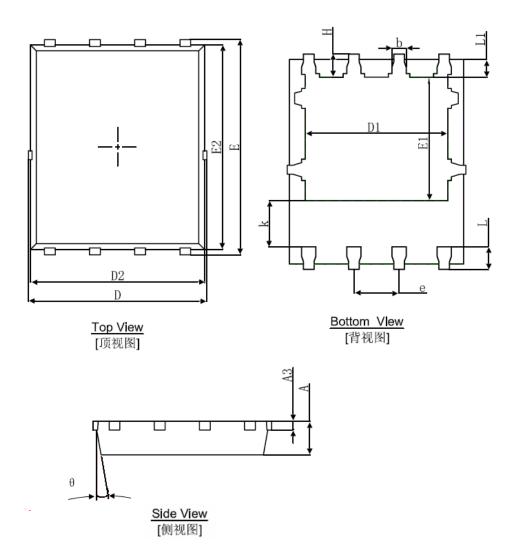
Figure 10 Power De-rating



**Figure 11 Normalized Maximum Transient Thermal Impedance** 



# **DFN5X6-8L Package Information**



Symbol	Dimensions In Millimeters		Dimensions In Inches		
	Min.	Max.	Min.	Max.	
Α	0.900	1.000	0.035	0.039	
A3	0.254	REF.	0.010	REF.	
D	4.944	5.096	0.195	0.201	
E	5.974	6.126	0.235	0.241	
D1	3.910	4.110	0.154	0.162	
E1	3.375	3.575	0.133	0.141	
D2	4.824	4.976	0.190	0.196	
E2	5.674	5.826	0.223	0.229	
k	1.190	1.390	0.047	0.055	
b	0.350	0.450	0.014	0.018	
е	1.270TYP.		0.050	TYP.	
L	0.559	0.711	0.022	0.028	
L1	0.424	0.576	0.017	0.023	
Н	0.574	0.726	0.023	0.029	
θ	8°	12°	8°	12°	



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