

## Description

The HM20N15K uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

## General Features

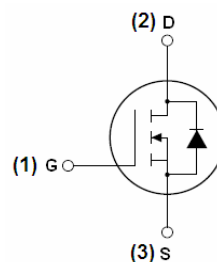
- $V_{DS} = 150V, I_D = 20A$   
 $R_{DS(ON)} < 85m\Omega @ V_{GS} = 10V$  (Typ: 70m $\Omega$ )
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation

## Application

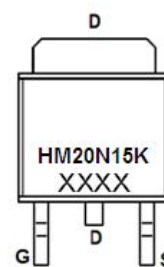
- Boost converters
- LED backlighting
- Uninterruptible power supply

**100% UIS TESTED!**

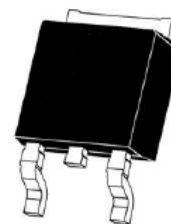
**100%  $\Delta V_{ds}$  TESTED!**



Schematic diagram



Marking and pin assignment



TO-252-2L top view

## Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM20N15K	HM20N15K	TO-252-2L	-	-	-

## Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Limit	Unit
$V_{DS}$	Drain-Source Voltage	150	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current-Continuous	20	A
$I_D(100^\circ C)$	Drain Current-Continuous( $T_C = 100^\circ C$ )	14	A
$I_{DM}$	Pulsed Drain Current	40	A
$P_D$	Maximum Power Dissipation	75	W
	Derating factor	0.5	W/ $^\circ C$
$E_{AS}$	Single pulse avalanche energy <sup>(Note 5)</sup>	200	mJ
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 To 175	$^\circ C$

## Thermal Characteristic

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	2.0	$^\circ C/W$
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**Electrical Characteristics ( $T_C=25^\circ\text{C}$  unless otherwise noted)**

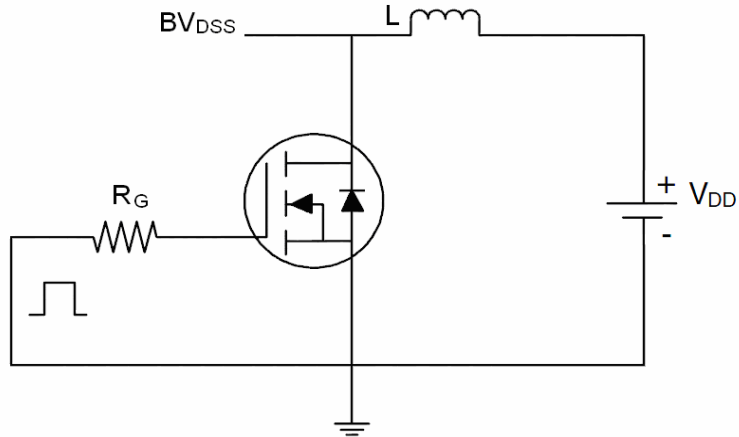
Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	150	165	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=150V, V_{GS}=0V$	-	-	1	$\mu A$
$I_{GSS}$	Gate-Body Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics (Note 3)</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3.4	4	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	$V_{GS}=10V, I_D=10A$	-	70	85	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=5V, I_D=10A$	-	20	-	S
<b>Dynamic Characteristics (Note 4)</b>						
$C_{iss}$	Input Capacitance	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0MHz$	-	2000	-	PF
$C_{oss}$	Output Capacitance		-	290	-	PF
$C_{rss}$	Reverse Transfer Capacitance		-	180	-	PF
<b>Switching Characteristics (Note 4)</b>						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=75V, R_L=5\Omega$ $V_{GS}=10V, R_{GEN}=3\Omega$	-	10.5	-	nS
$t_r$	Turn-on Rise Time		-	5.5	-	nS
$t_{d(off)}$	Turn-Off Delay Time		-	14.5	-	nS
$t_f$	Turn-Off Fall Time		-	3	-	nS
$Q_g$	Total Gate Charge	$V_{DS}=75V, I_D=10A,$ $V_{GS}=10V$	-	17	-	nC
$Q_{gs}$	Gate-Source Charge		-	4	-	nC
$Q_{gd}$	Gate-Drain Charge		-	4.4	-	nC
<b>Drain-Source Diode Characteristics</b>						
$V_{SD}$	Diode Forward Voltage (Note 3)	$V_{GS}=0V, I_S=20A$	-	-	1.2	V
$I_S$	Diode Forward Current (Note 2)	-	-	-	20	A
$t_{rr}$	Reverse Recovery Time	$T_J = 25^\circ\text{C}, I_F = 10A$ $di/dt = 100A/\mu s$ (Note 3)	-	32	-	nS
$Q_{rr}$	Reverse Recovery Charge		-	53	-	nC
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

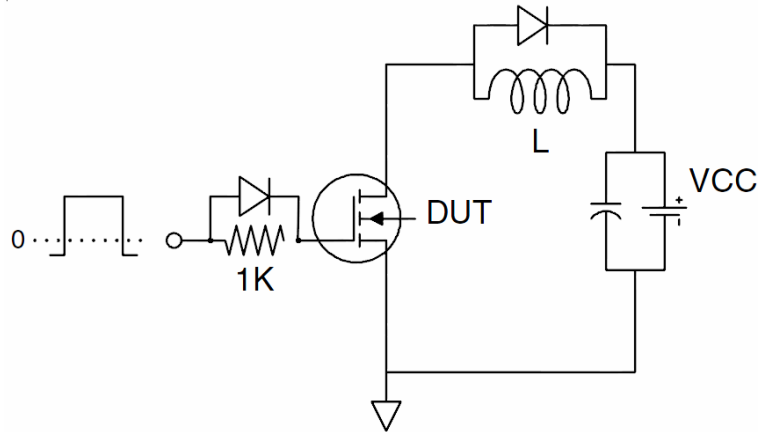
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition:  $T_J=25^\circ\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

**Test Circuit**

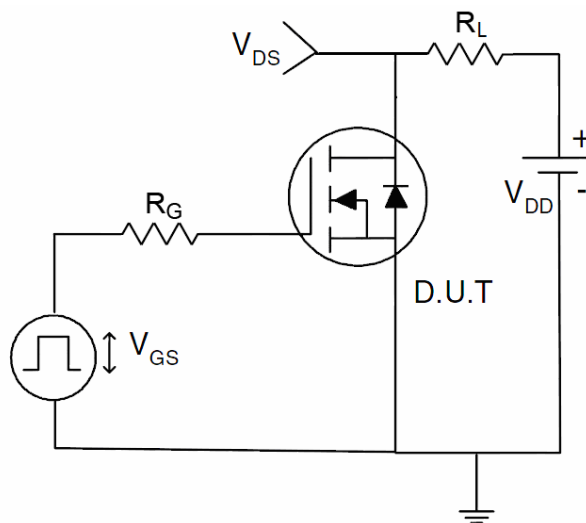
**1) E<sub>AS</sub> Test Circuit**



**2) Gate Charge Test Circuit**



**3) Switch Time Test Circuit**



Typical Electrical and Thermal Characteristics (Curves)

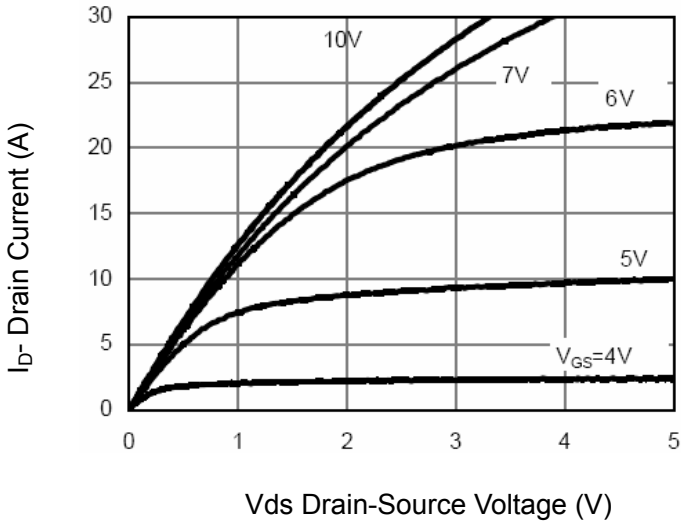


Figure 1 Output Characteristics

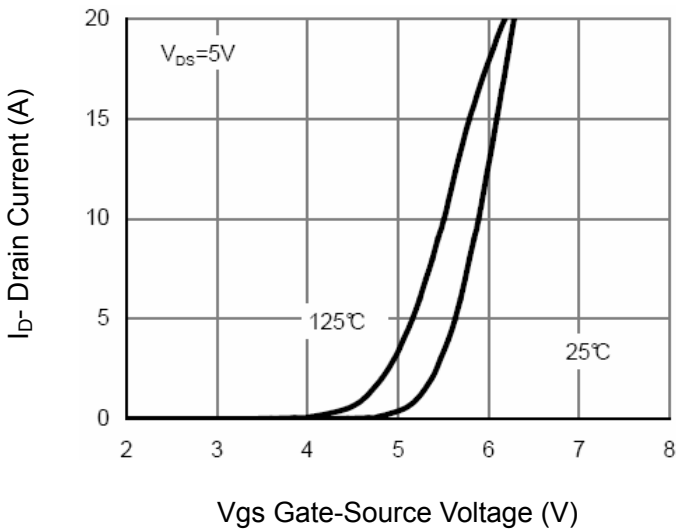


Figure 2 Transfer Characteristics

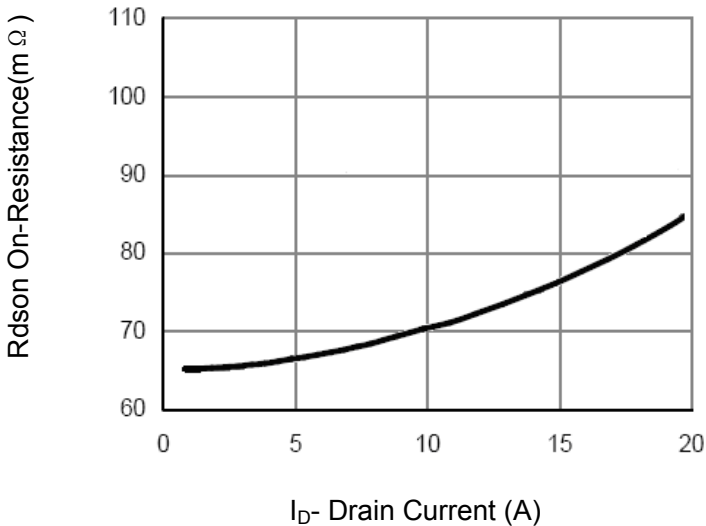


Figure 3 Rdson- Drain Current

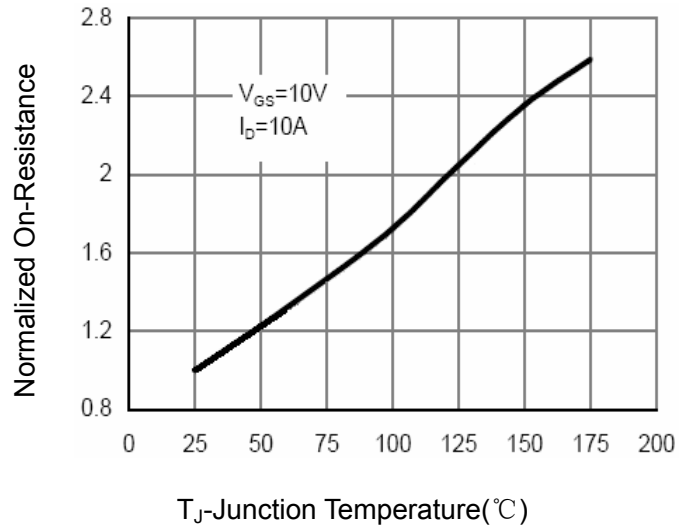


Figure 4 Rdson-Junction Temperature

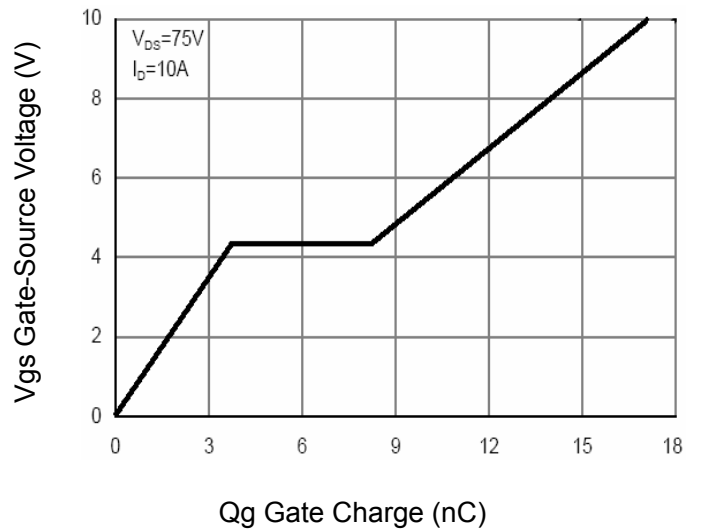


Figure 5 Gate Charge

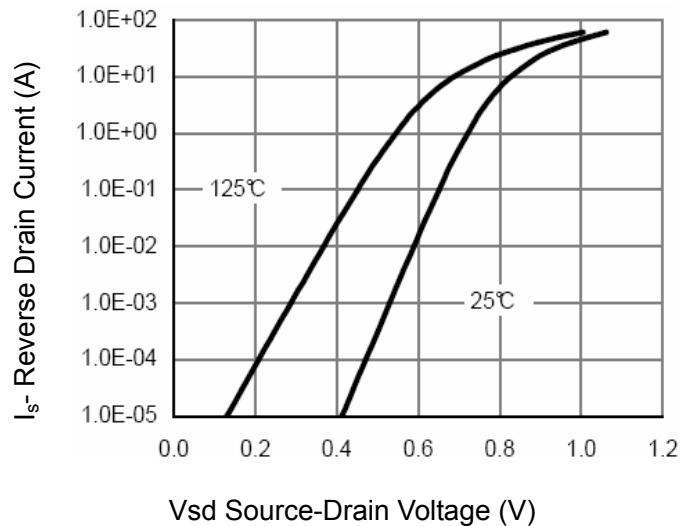


Figure 6 Source- Drain Diode Forward

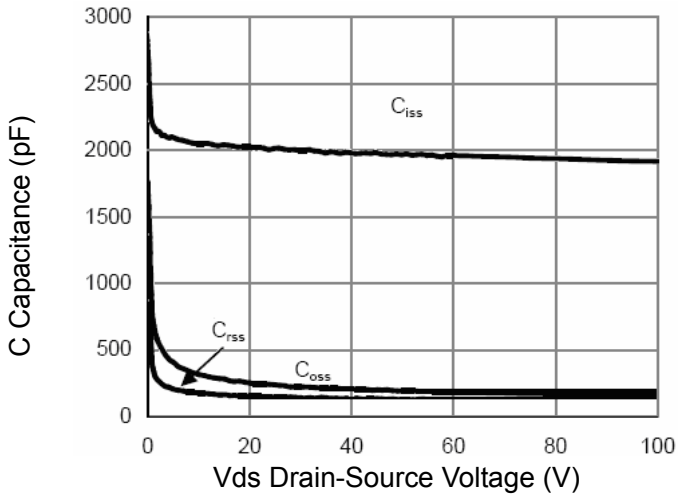


Figure 7 Capacitance vs Vds

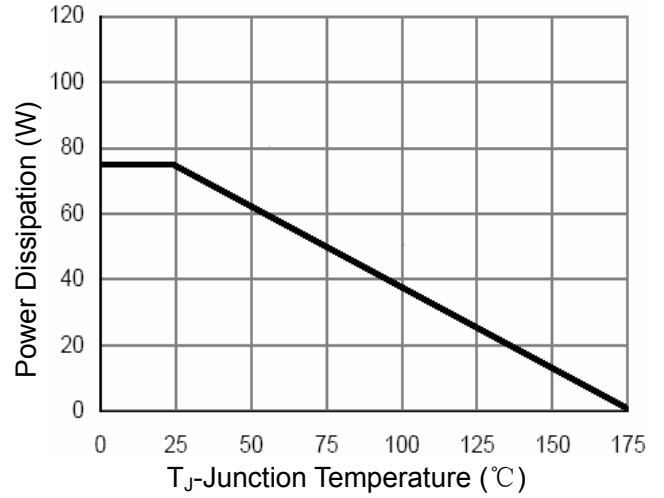


Figure 9 Power De-rating

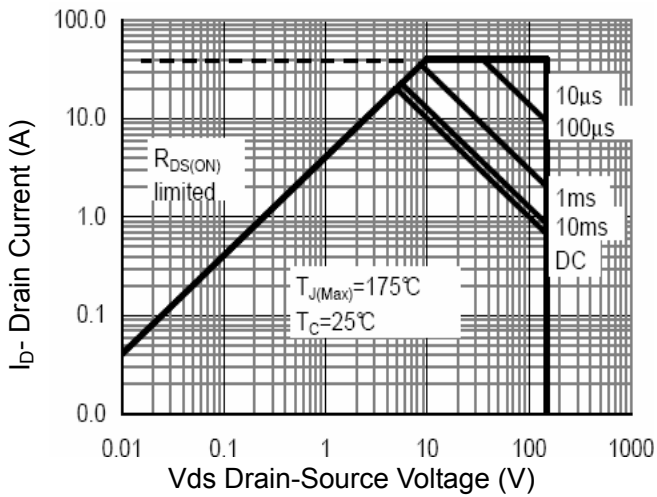


Figure 8 Safe Operation Area

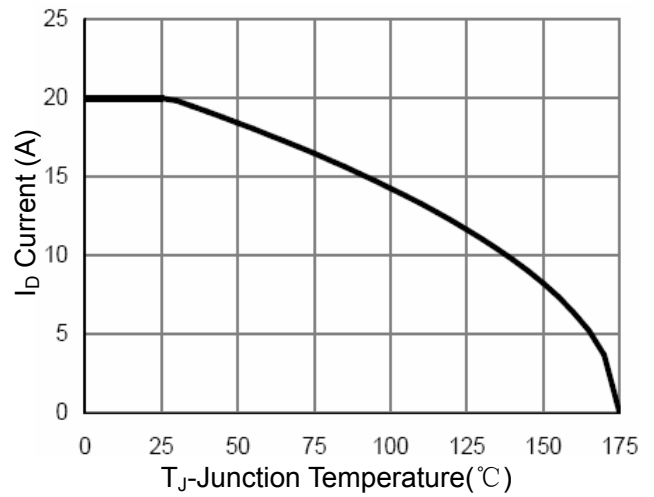


Figure 10 Id Current- Junction Temperature

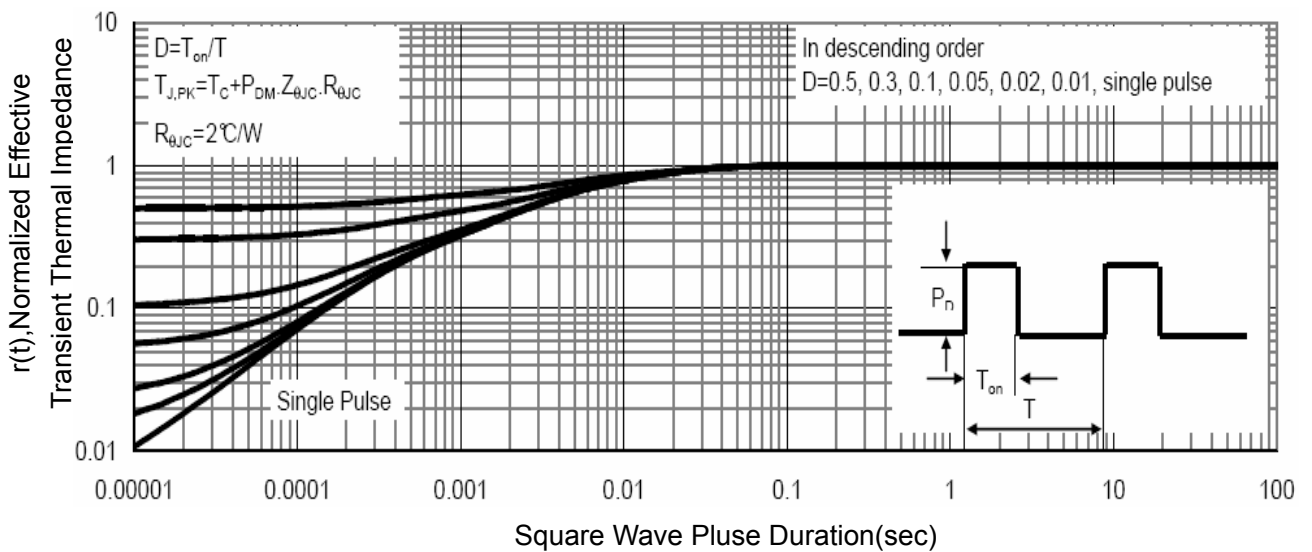
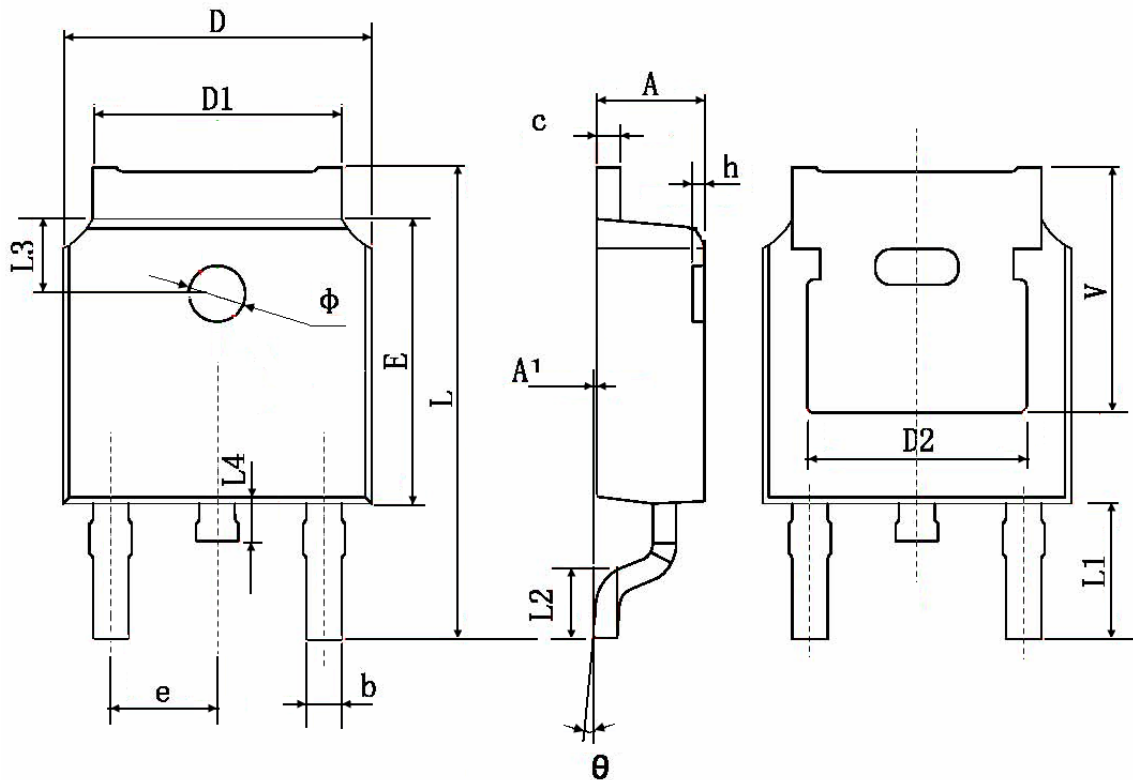


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	0.483 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	