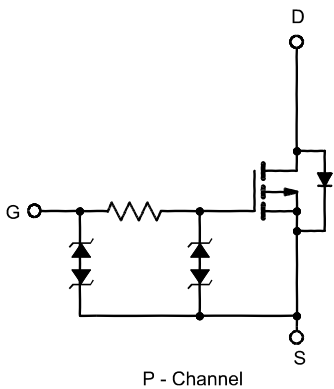


### GENERAL DESCRIPTION

The PT GEFÖÜ is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

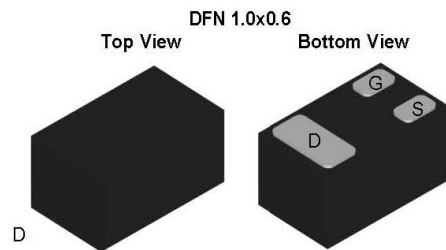
### APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System



### FEATURES

- $R_{DS(ON)} = 0.48\Omega @ V_{GS} = -4.5V$
- $R_{DS(ON)} = 0.67\Omega @ V_{GS} = -2.5V$
- $R_{DS(ON)} = 0.95\Omega @ V_{GS} = -1.8V$
- $R_{DS(ON)} = 2.20\Omega @ V_{GS} = -1.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- Capable doing Cu wire bonding



### Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

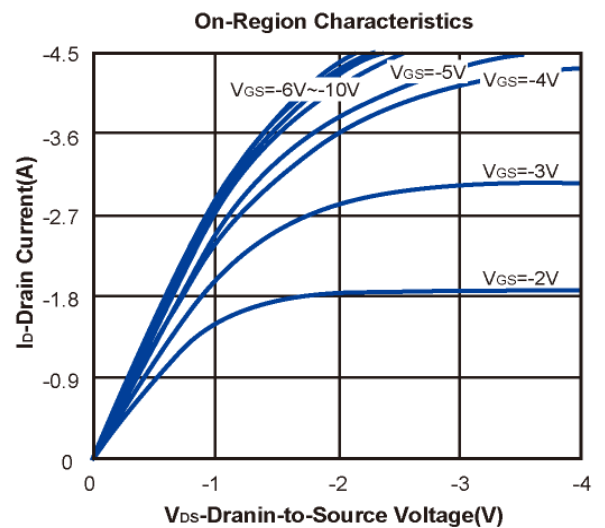
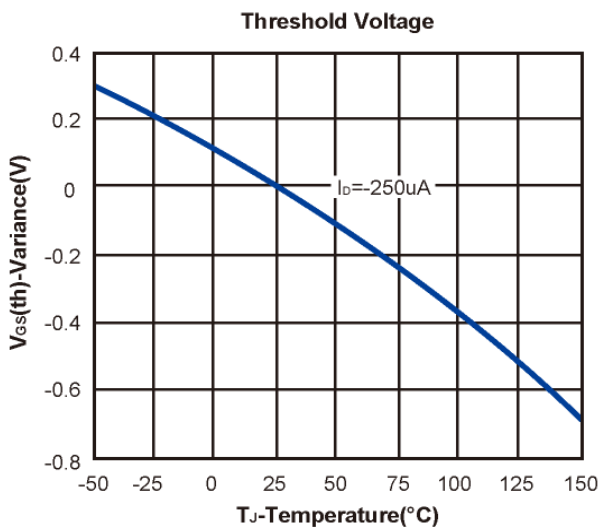
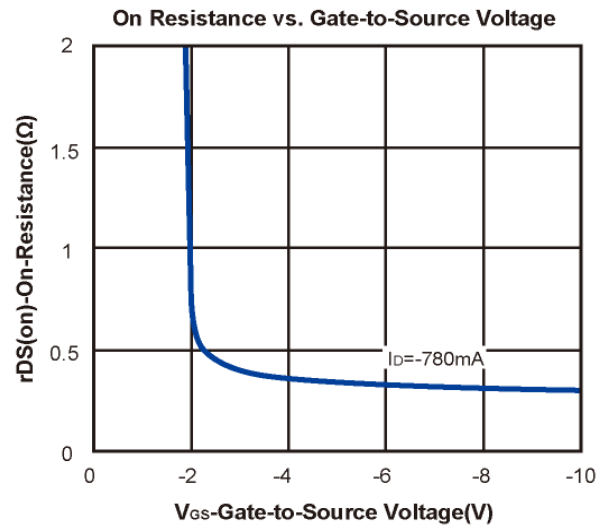
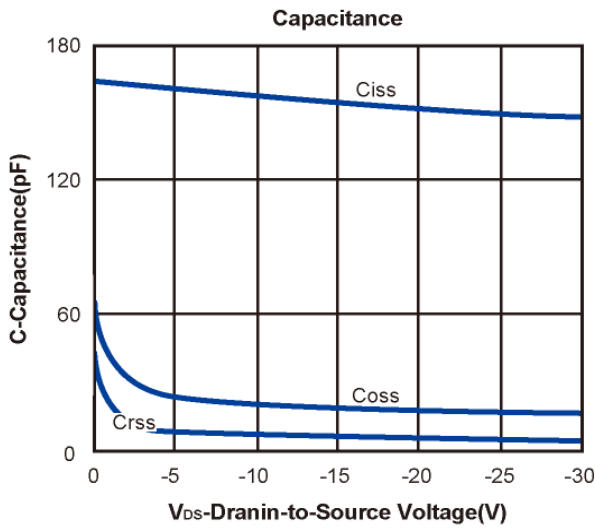
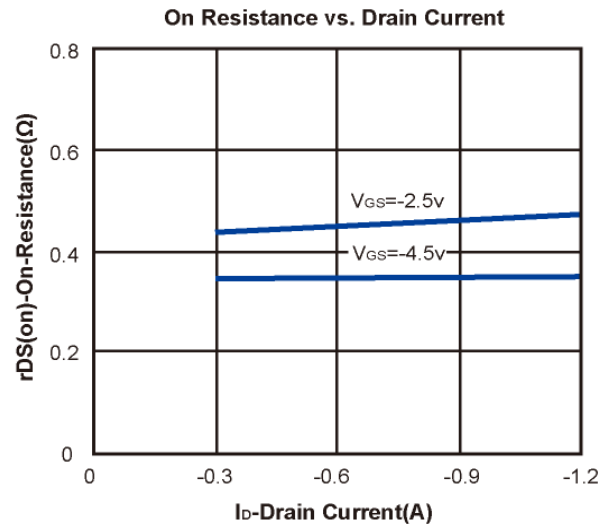
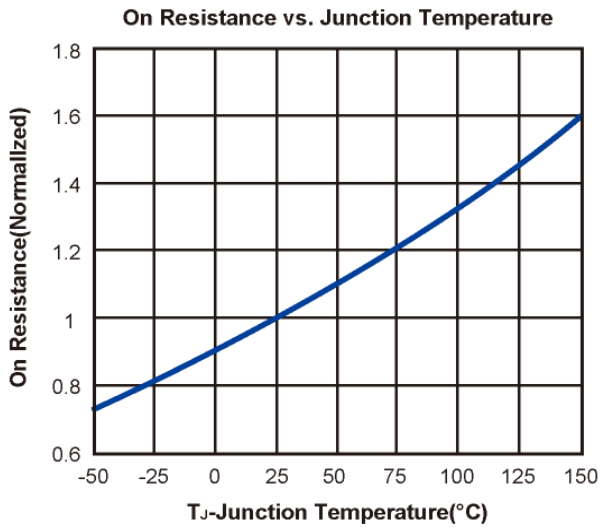
Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V <sub>DS</sub>	-20	V
Gate-Source Voltage	V <sub>GS</sub>	±6	V

**Electrical Characteristics** ( $T_J = 25^\circ\text{C}$  Unless Otherwise Specified)

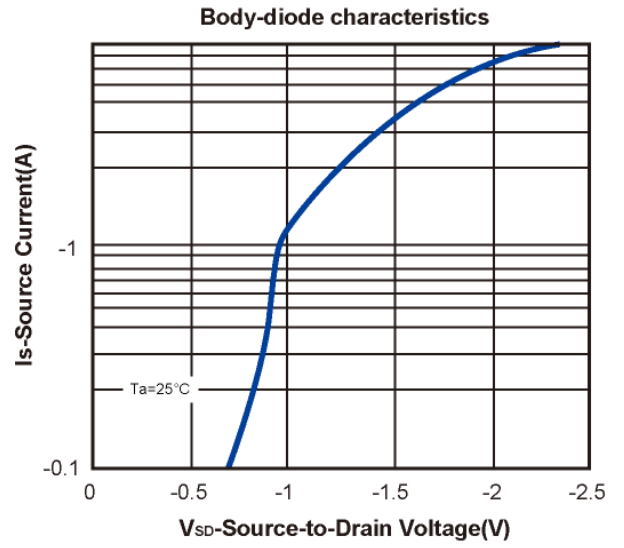
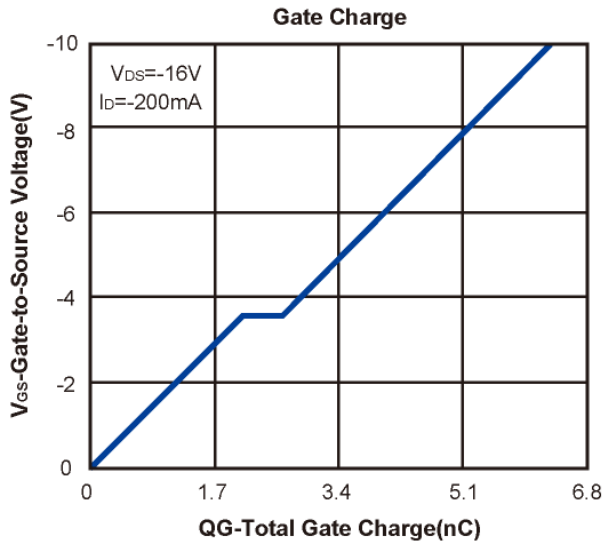
Symbol	Parameter	Limit	Min	Typ	Max	Unit
<b>STATIC</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-20			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.45		-1.2	V
$I_{GSS}$	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 4.5V$			$\pm 10$	$\mu A$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-16V, V_{GS}=0V$			-1	$\mu A$
$R_{DS(on)}$	Drain-Source On-Resistance <sup>a</sup>	$V_{GS}=-4.5V, I_D=-780mA$		0.35	0.48	$\Omega$
		$V_{GS}=-2.5V, I_D=-660mA$		0.44	0.67	
		$V_{GS}=-1.8V, I_D=-100mA$		0.55	0.95	
		$V_{GS}=-1.5V, I_D=-100mA$		0.78	2.20	
$V_{SD}$	Diode Forward Voltage	$I_S=-350mA, V_{GS}=0V$		-0.8	-1.2	V
<b>DYNAMIC</b>						
$C_{iss}$	Input Capacitance	$V_{DS}=-16V, V_{GS}=0V, f=1MHz$		152		pF
$C_{oss}$	Output Capacitance			18.5		
$C_{rss}$	Reverse Transfer Capacitance			6		
$Q_g$	Total Gate Charge	$V_{DS}=-16V, V_{GS}=-4.5V, I_D=-200mA$		2.8		nC
$Q_{gs}$	Gate-Source Charge			2.1		
$Q_{gd}$	Gate-Drain Charge			0.5		
$t_{d(on)}$	Turn-On Delay Time	$V_{DD}=-10V, R_L=50\Omega$ $V_{GEN}=-5V, R_G=10\Omega$ $I_D=-200mA$		51.3		ns
$t_r$	Turn-On Rise Time			24.2		
$t_{d(off)}$	Turn-Off Delay Time			246		
$t_f$	Turn-Off Fall Time			81.2		

- Notes: a. Based on Eutectic paste and bond wire Cu wire 1mil×1(S), Cu wire 1mil×1(G) on each die of SOT-523 package.  
 b. Pulse test; pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .  
 c. H&M SEMI reserves the right to improve product design, functions and reliability without notice.

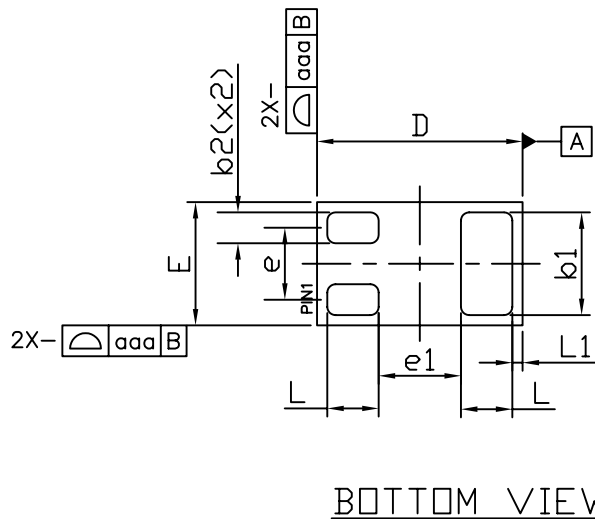
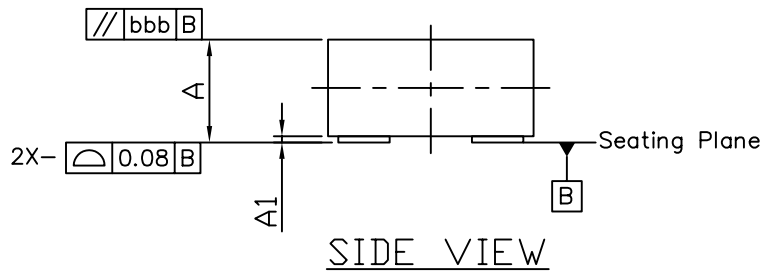
**Typical Characteristics (T<sub>J</sub> =25°C Noted)**



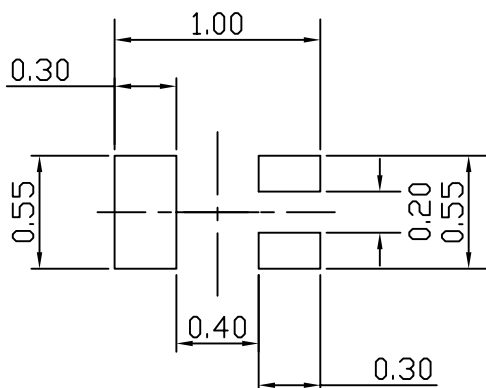
**Typical Characteristics (T<sub>J</sub> =25°C Noted)**



**DFN1.0X0.6-3L**



**RECOMMENDED LAND PATTERN**



UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.52	0.55	0.019	0.020	0.022
A1	0.00	0.03	0.05	0.000	0.001	0.002
b1	0.45	0.50	0.55	0.018	0.020	0.022
b2	0.10	0.15	0.20	0.004	0.006	0.008
D	0.95	1.00	1.075	0.037	0.039	0.042
E	0.55	0.60	0.675	0.022	0.024	0.027
e	---	0.35	---	---	0.014	---
e1	---	0.40	---	---	0.016	---
L	0.20	0.25	0.30	0.008	0.010	0.012
L1	---	0.05	---	---	0.002	---
aaa	0.15			0.006		
bbb	0.05			0.002		

**NOTE**

1. ALL DIMENSION ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.