

GENERAL DESCRIPTION

The HM2309 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

FEATURES

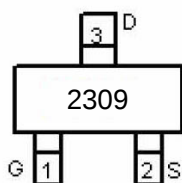
- $R_{DS(ON)} \leq 215m\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} \leq 260m\Omega @ V_{GS} = -4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- Capable doing Cu wire bonding

APPLICATIONS

- Power Management
- Portable Equipment
- Battery Powered System
- Load Switch

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

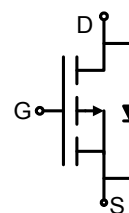
Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	±20	V



Marking and pin Assignment



SOT-23-3L top view



Schematic diagram

Electrical Characteristics (T_j = 25°C Unless Otherwise Specified)

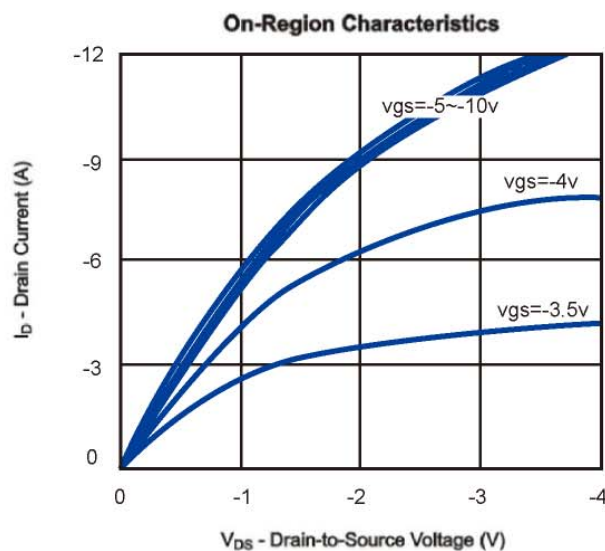
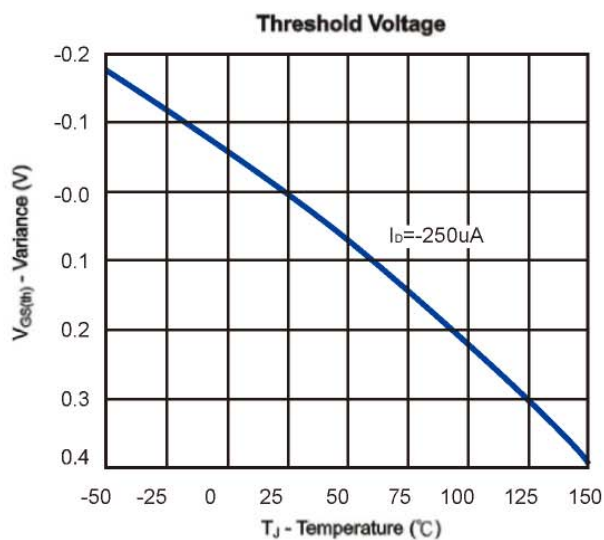
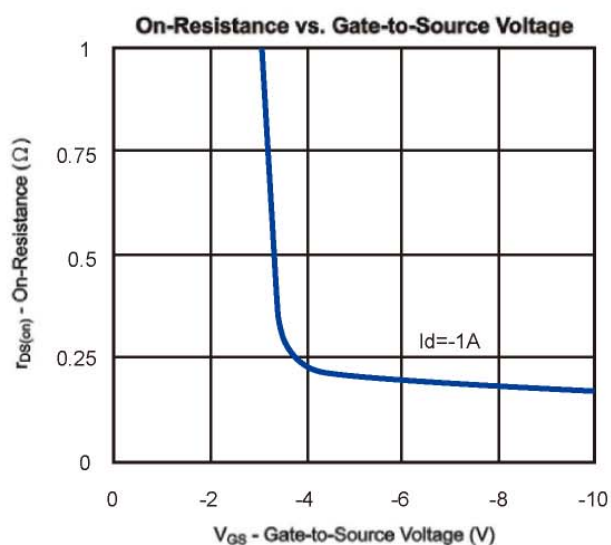
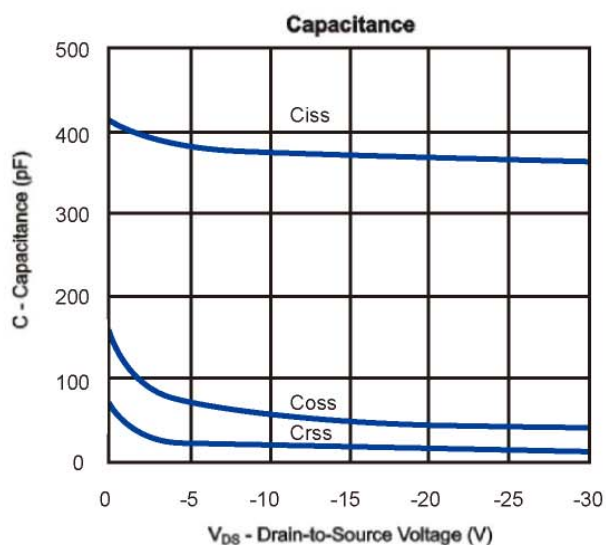
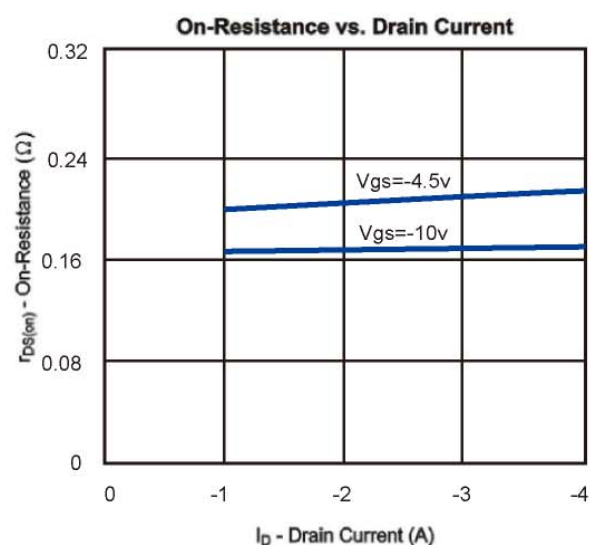
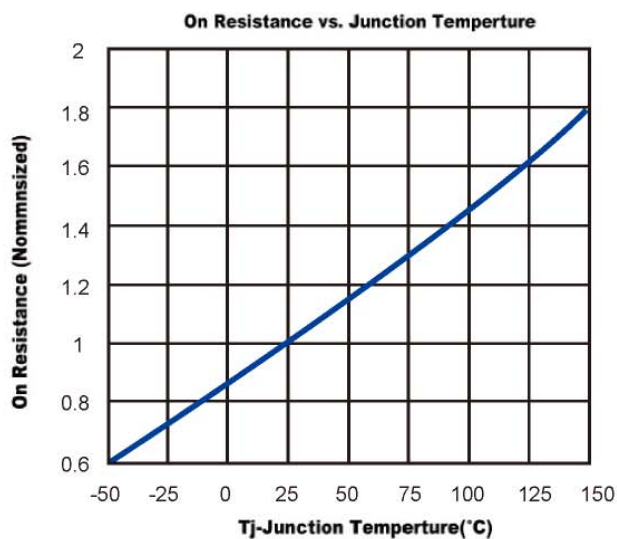
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250 μA	-60			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250 μA	-1		-3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-60V, V _{GS} =0V			-10	μA
R _{DS(ON)}	Drain-Source On-Resistance	V _{GS} =-10V, I _D = -1.8A		170	215	mΩ
		V _{GS} =-4.5V, I _D = -1.4A		200	260	
V _{SD}	Diode Forward Voltage	I _S =-1.2A, V _{GS} =0V			-1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =-48V, V _{GS} =-4.5V, I _D =-1A		6.3		nC
Q _{gs}	Gate-Source Charge			2.3		
Q _{gd}	Gate-Drain Charge			1.8		
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz		9.8		Ω
t _{d(on)}	Turn-On Delay Time	V _{DS} =-30V, R _L =30Ω R _{GEN} =3.3Ω, V _{GS} =-10V I _D =-1A		20		ns
t _r	Turn-On Rise Time			33.1		
t _{d(off)}	Turn-Off Delay Time			5.2		
t _f	Turn-Off Fall Time			3.8		
C _{iss}	Input Capacitance	V _{DS} =-25V, V _{GS} =0V, f=1MHz		364		pF
C _{oss}	Output Capacitance			41		
C _{rss}	Reverse Transfer Capacitance			12		

Notes: a. Based on epoxy or solder paste and bond wire Au or Cu 2mil×2(S), Au or Cu 2mil×1 (G) on each die of SOT-23 (SC-59) package.

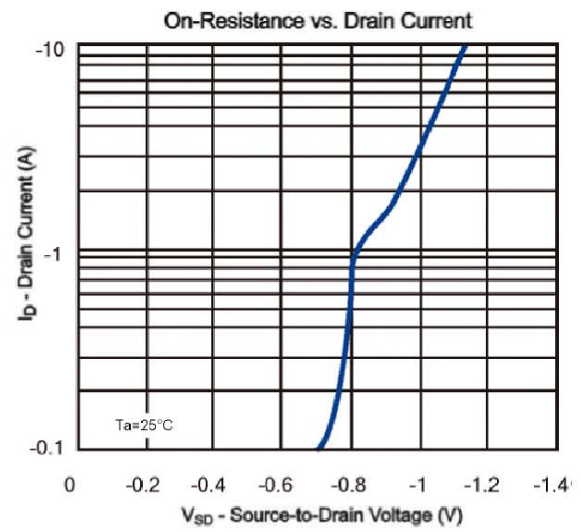
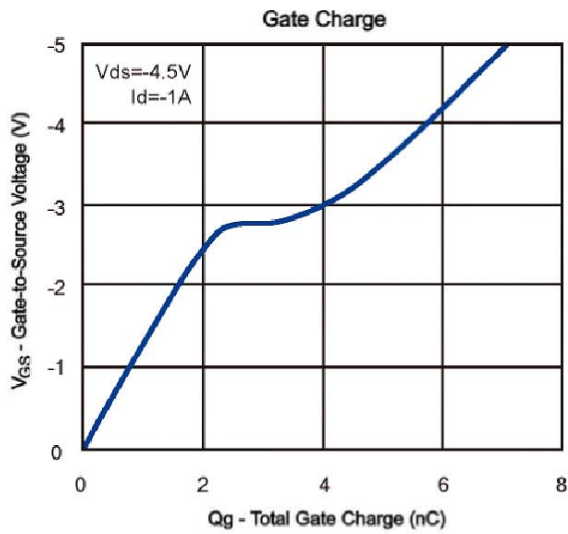
b. Pulse test; pulse width ≤ 300us, duty cycle ≤ 2%.

c. H&M SEMI reserves the right to improve product design, functions and reliability without notice.

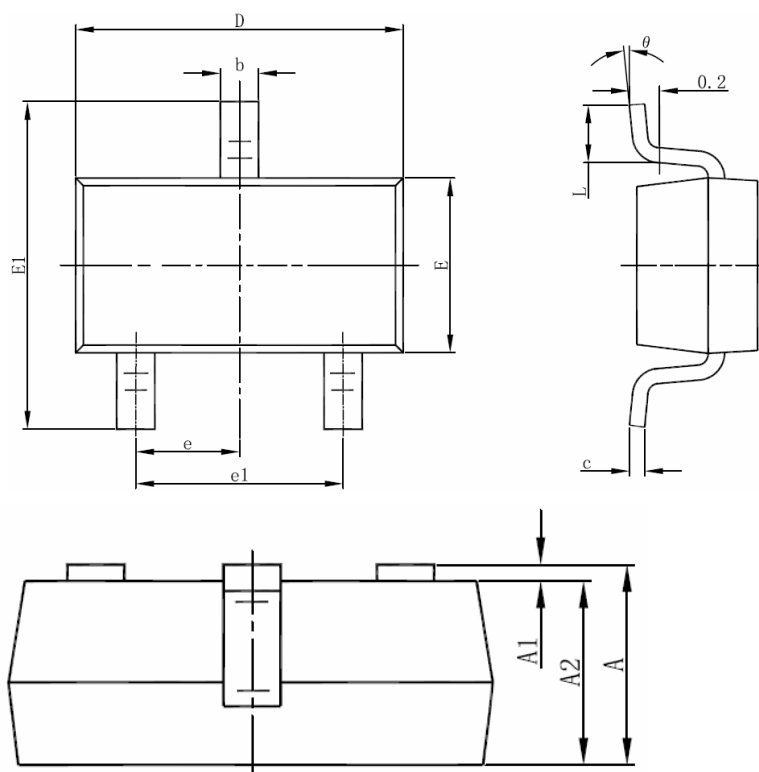
Typical Characteristics (T_J = 25°C Noted)



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SOT-23-3L PACKAGE INFORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

NOTES

1. All dimensions are in millimeters.
2. Tolerance $\pm 0.10\text{mm}$ (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.