

**N-Channel 40V(D-S) MOSFET**

**GENERAL DESCRIPTION**

The HM2318A is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

**FEATURES**

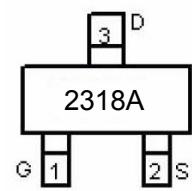
- $R_{DS(ON)} \leq 28m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 38m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- Capable doing Cu wire bonding

**APPLICATIONS**

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

**Absolute Maximum Ratings ( $T_A=25^\circ C$  Unless Otherwise Noted)**

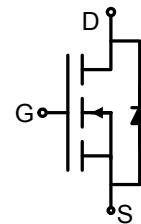
Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V



Marking and pin Assignment



SOT-23-3L top view



Schematic diagram

**N-Channel 40V(D-S) MOSFET**

**Electrical Characteristics ( $T_j = 25^\circ\text{C}$  Unless Otherwise Specified)**

Symbol	Parameter	Limit	Min	Typ	Max	Unit
<b>STATIC</b>						
$\text{BV}_{\text{DSS}}$	Drain-Source Breakdown Voltage	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_d=250 \mu\text{A}$	40			V
$\text{V}_{\text{GS(th)}}$	Gate Threshold Voltage	$\text{V}_{\text{DS}}=\text{V}_{\text{GS}}, \text{I}_d=250 \mu\text{A}$	1.0		2.5	V
$\text{I}_{\text{GSS}}$	Gate Body Leakage	$\text{V}_{\text{DS}}=0\text{V}, \text{V}_{\text{GS}}=\pm 20\text{V}$			$\pm 100$	nA
$\text{I}_{\text{DSS}}$	Zero Gate Voltage Drain Current	$\text{V}_{\text{DS}}=40\text{V}, \text{V}_{\text{GS}}=0\text{V}$			1	$\mu\text{A}$
$\text{R}_{\text{DS(ON)}}$	Drain-Source On-Resistance	$\text{V}_{\text{GS}}=10\text{V}, \text{I}_d= 5.0\text{A}$			28	$\text{m}\Omega$
		$\text{V}_{\text{GS}}=4.5\text{V}, \text{I}_d= 3.5\text{A}$			38	
$\text{V}_{\text{SD}}$	Diode Forward Voltage	$\text{I}_s=1\text{A}$		0.8	1.2	V
<b>DYNAMIC</b>						
$\text{Q}_g$	Total Gate Charge	$\text{V}_{\text{DS}}=20\text{V}, \text{V}_{\text{GS}}=10\text{V}, \text{I}_d=5\text{A}$		16		nC
$\text{Q}_g$	Total Gate Charge	$\text{V}_{\text{DS}}=20\text{V}, \text{V}_{\text{GS}}=4.5\text{V}, \text{I}_d=5\text{A}$		8.2		
$\text{Q}_{\text{gs}}$	Gate-Source Charge			3.6		
$\text{Q}_{\text{gd}}$	Gate-Drain Charge			3.9		
$\text{C}_{\text{iss}}$	Input capacitance	$\text{V}_{\text{DS}}=20\text{V}, \text{V}_{\text{GS}}=0\text{V}, \text{f}=1\text{MHz}$		560		pF
$\text{C}_{\text{oss}}$	Output Capacitance			70		
$\text{C}_{\text{rss}}$	Reverse Transfer Capacitance			22		
$\text{R}_g$	Gate Resistance	$\text{f}=1\text{MHz}$		0.7		$\Omega$
$\text{t}_{\text{d(on)}}$	Turn-On Delay Time	$\text{V}_{\text{DD}}=20\text{V}, \text{R}_L = 20\Omega$ $\text{I}_d=1\text{A}, \text{V}_{\text{GEN}}=10\text{V}$ $\text{R}_G=1\Omega$		12		ns
$\text{t}_r$	Turn-On Rise Time			12		
$\text{t}_{\text{d(off)}}$	Turn-Off Delay Time			37		
$\text{t}_f$	Turn-Off Fall Time			4		

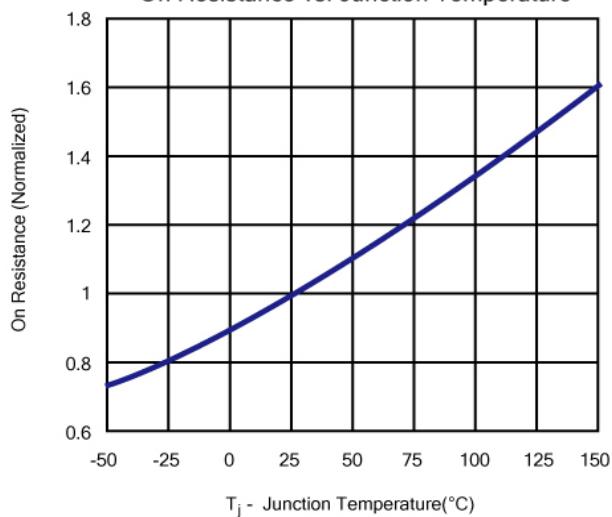
Notes: a. Based on epoxy or solder paste and bond wire Cu 2mil×3(S), Au 1mil ×1(G) on each die of SOT-23 package.

b. Pulse test; pulse width  $\leq 300\text{us}$ , duty cycle  $\leq 2\%$ .

c. H&M SEMI reserves the right to improve product design, functions and reliability without notice.

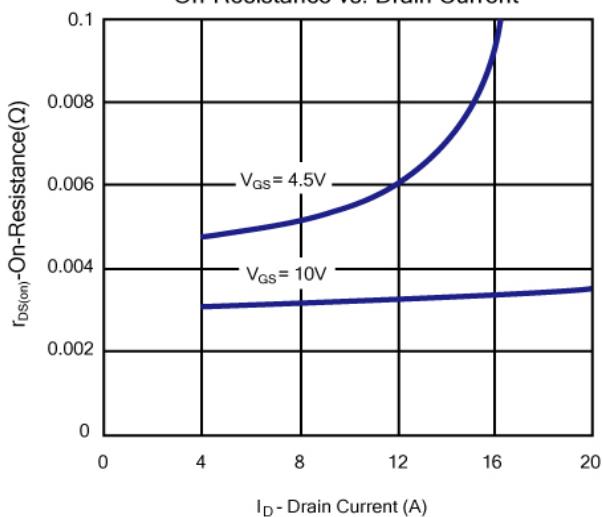
**Typical Characteristics (T<sub>J</sub> =25°C Noted)**

On Resistance vs. Junction Temperature

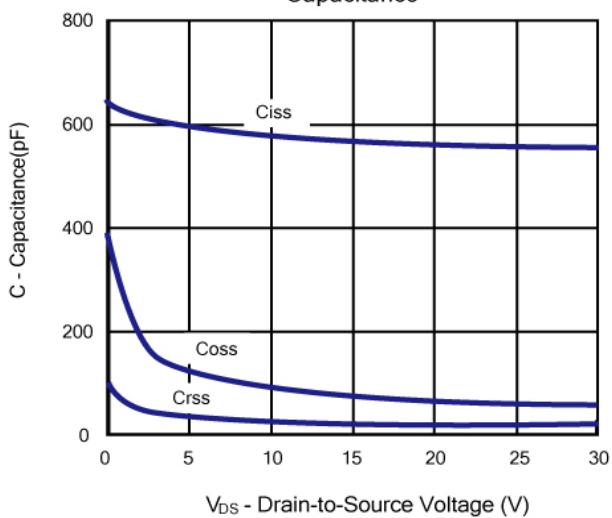


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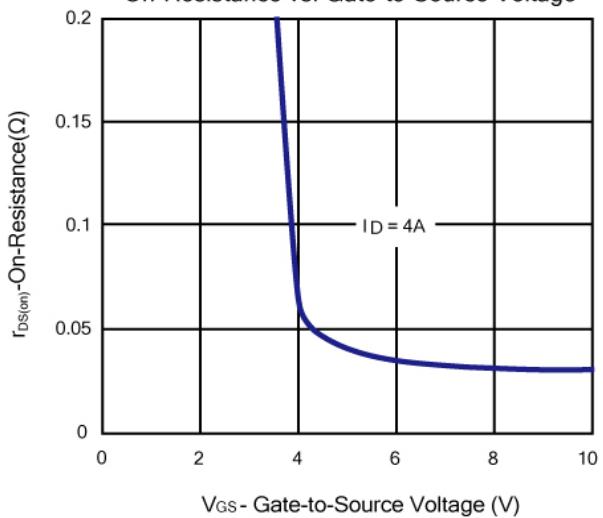
On-Resistance vs. Drain Current



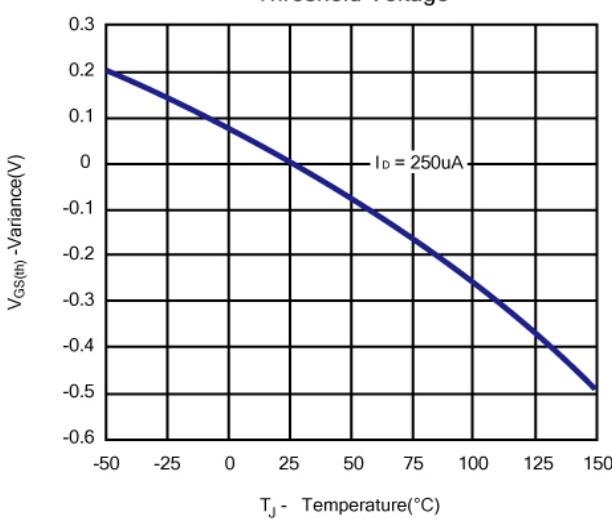
Capacitance



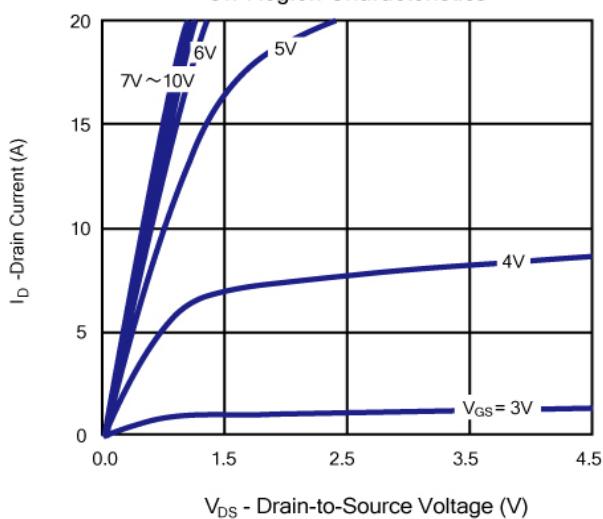
On-Resistance vs. Gate-to-Source Voltage



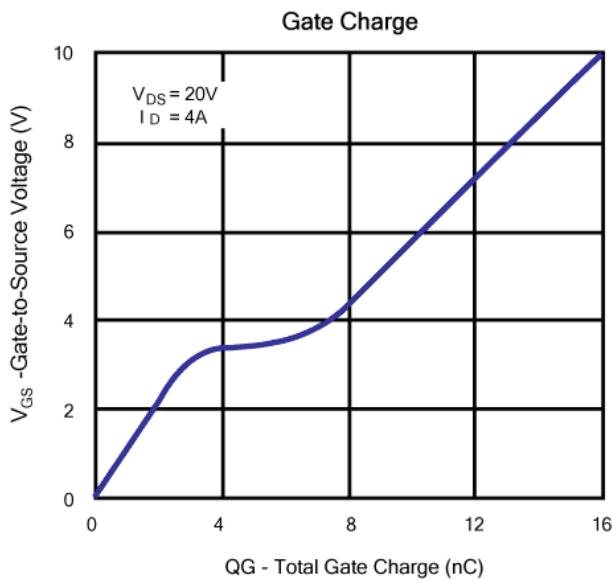
Threshold Voltage



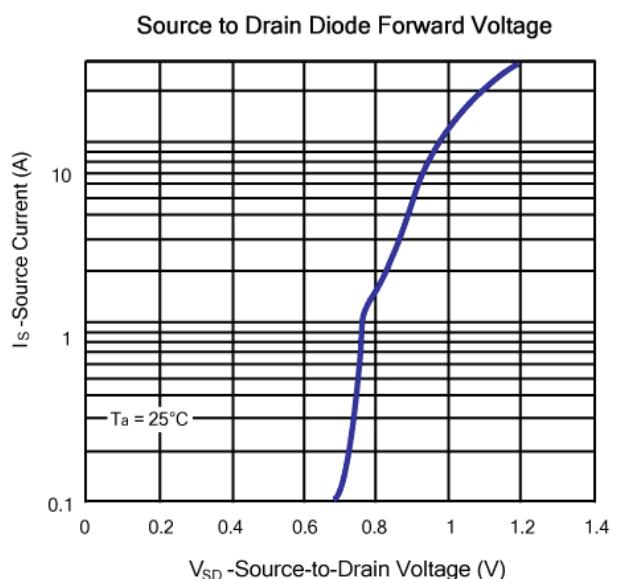
On-Region Characteristics



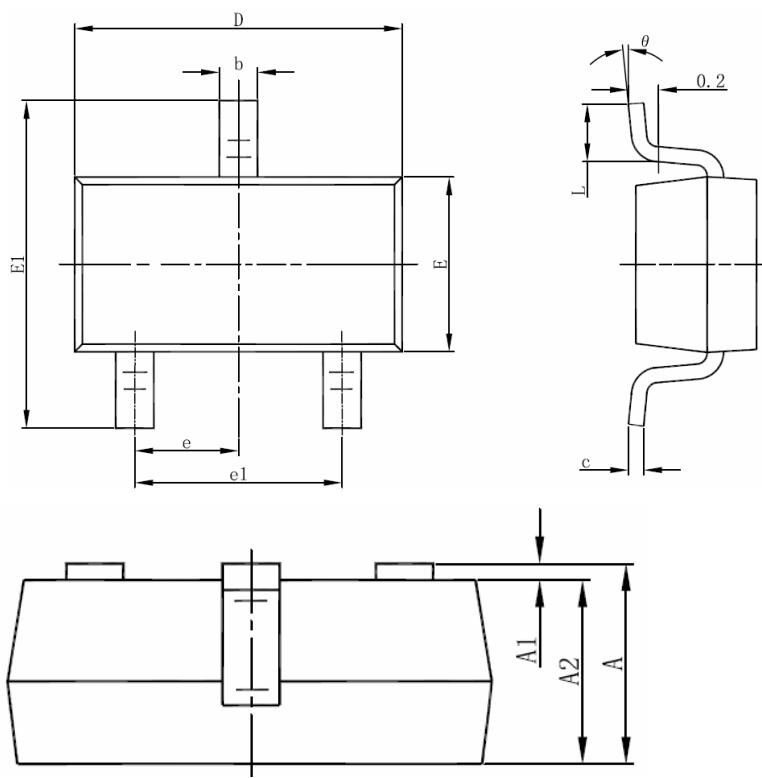
**Typical Characteristics ( $T_J = 25^\circ\text{C}$  Noted)**



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## SOT-23-3L PACKAGE INFORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

### NOTES

1. All dimensions are in millimeters.
2. Tolerance  $\pm 0.10$ mm (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.