

## P-Channel Enhancement Mode Power MOSFET

### Description

The HM25P06K uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge .This device is well suited for high current load applications.

## General Features

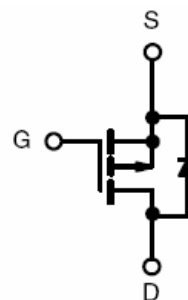
- $V_{DS} = -60V, I_D = -25A$   
 $R_{DS(ON)} < 45m\Omega @ V_{GS} = -10V$
- High density cell design for ultra low  $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation

## Application

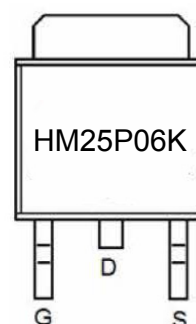
- High side switch for full bridge converter
- DC/DC converter for LCD display

**100% UIS TESTED!**

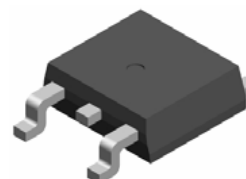
**100% AVds TESTED!**



### Schematic diagram



### Marking and pin assignment



**TO-252-2L top view**

## Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM25P06K	HM25P06K	TO-252-2L	-	-	-

**Absolute Maximum Ratings (T<sub>C</sub>=25°C unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	-25	A
Drain Current-Continuous( $T_C=100^{\circ}C$ )	$I_D(100^{\circ}C)$	-17.7	A
Pulsed Drain Current	$I_{DM}$	-75	A
Maximum Power Dissipation	$P_D$	90	W
Derating factor		0.72	W/ $^{\circ}C$

Single pulse avalanche energy <sup>(Note 5)</sup>	E <sub>AS</sub>	300	mJ
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 To 150	°C

## Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	1.4	$^{\circ}\text{C/W}$
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### Electrical Characteristics (T<sub>C</sub>=25°C unless otherwise noted)

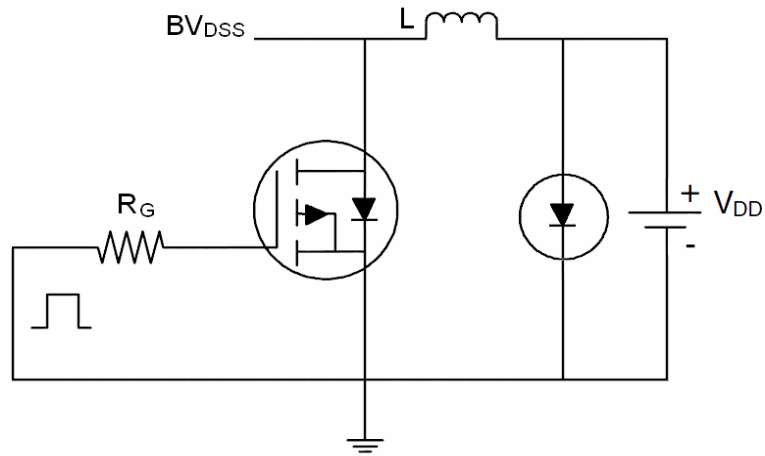
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-60	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-60V, V_{GS}=0V$	-	-	-1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-2	-2.9	-3.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-20A$	-	39	45	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=-10V, I_D=-10A$	-	25	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	$C_{ISS}$	$V_{DS}=-30V, V_{GS}=0V,$ $F=1.0MHz$	-	3430	-	PF
Output Capacitance	$C_{OSS}$		-	391	-	PF
Reverse Transfer Capacitance	$C_{RSS}$		-	272	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-30V, R_L=1.5\Omega,$ $V_{GS}=-10V, R_G=3\Omega$	-	12	-	nS
Turn-on Rise Time	$t_r$		-	15	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	38	-	nS
Turn-Off Fall Time	$t_f$		-	15	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=-30, I_D=-20A,$ $V_{GS}=-10V$	-	46		nC
Gate-Source Charge	$Q_{gs}$		-	9.5		nC
Gate-Drain Charge	$Q_{gd}$		-	10.5		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	$V_{SD}$	$V_{GS}=0V, I_S=-10A$	-		-1.2	V
Diode Forward Current (Note 2)	$I_S$		-	-	-25	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^{\circ}C, I_F = -10A$	-	47		nS
Reverse Recovery Charge	$Q_{rr}$	$di/dt = -100A/\mu s(Notes 3)$	-	53		nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

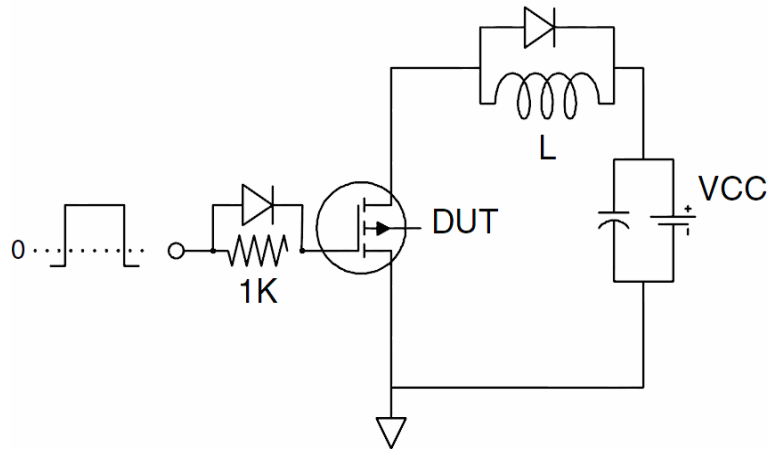
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5.  $E_{AS}$  condition:  $T_i=25^\circ C$ ,  $V_{DD}=20V$ ,  $V_{GS}=-10V$ ,  $L=1mH$ ,  $R_g=25\Omega$ ,  $I_{AS}=33A$

## Test Circuit

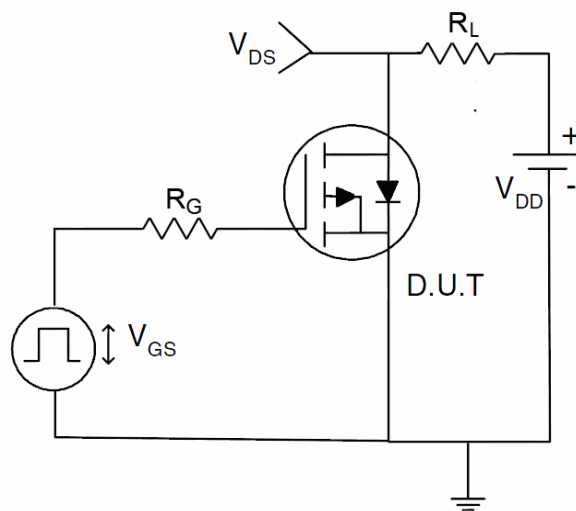
### 1) $E_{AS}$ Test Circuit



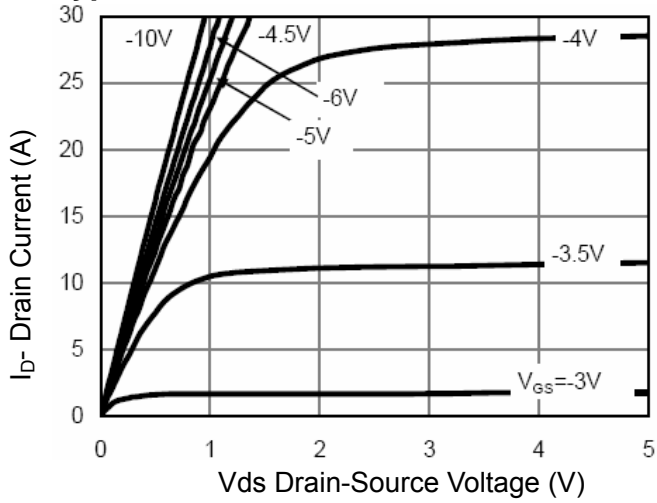
### 2) Gate Charge Test Circuit



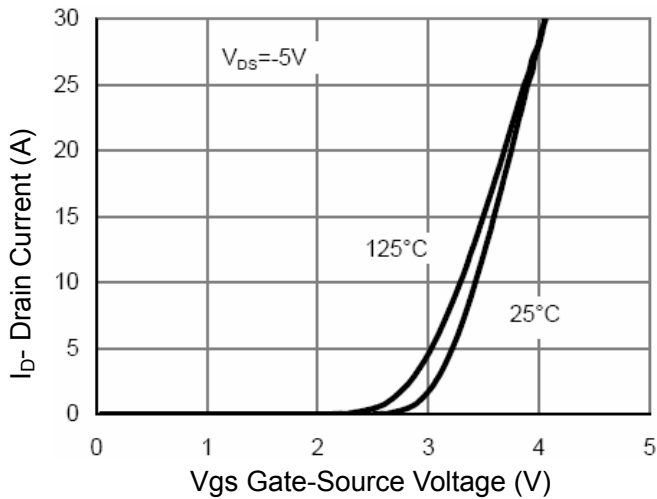
### 3) Switch Time Test Circuit



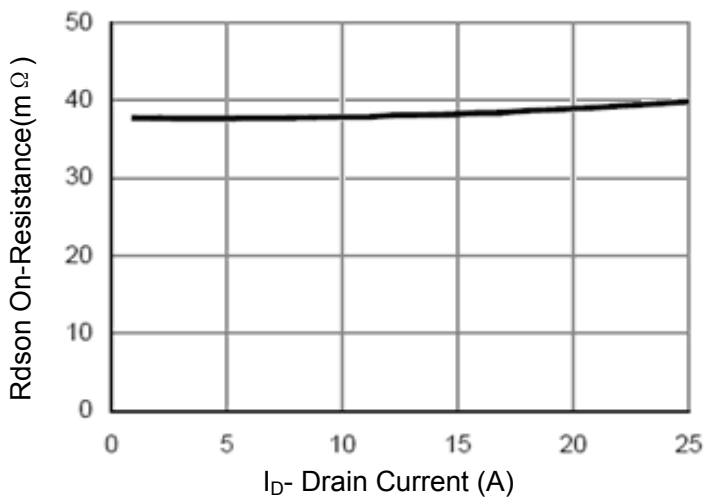
## Typical Electrical and Thermal Characteristics (Curves)



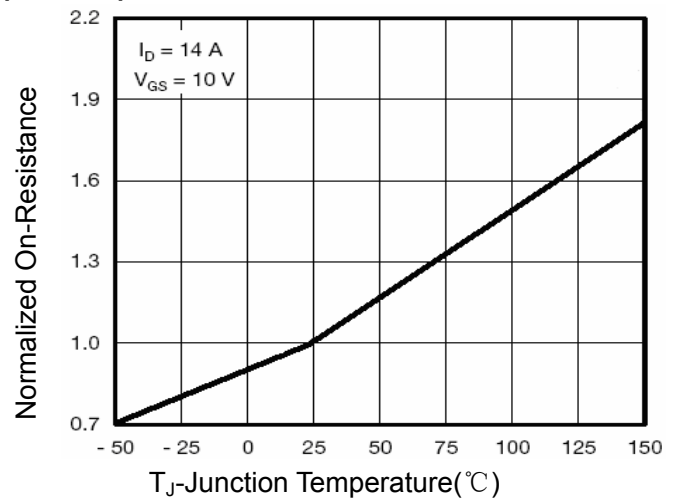
**Figure 1 Output Characteristics**



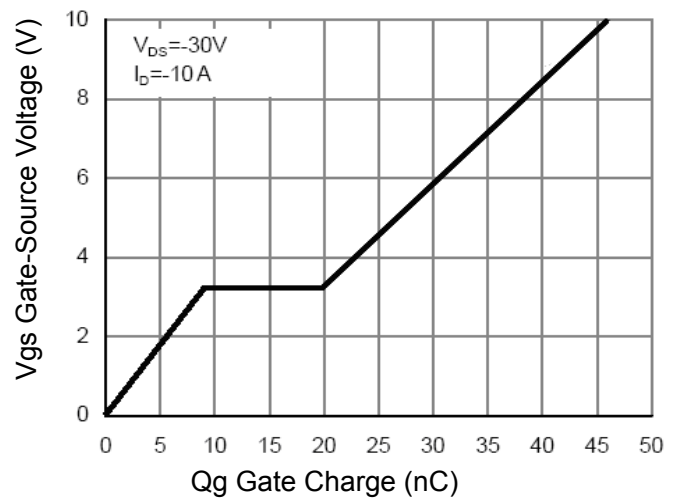
**Figure 2 Transfer Characteristics**



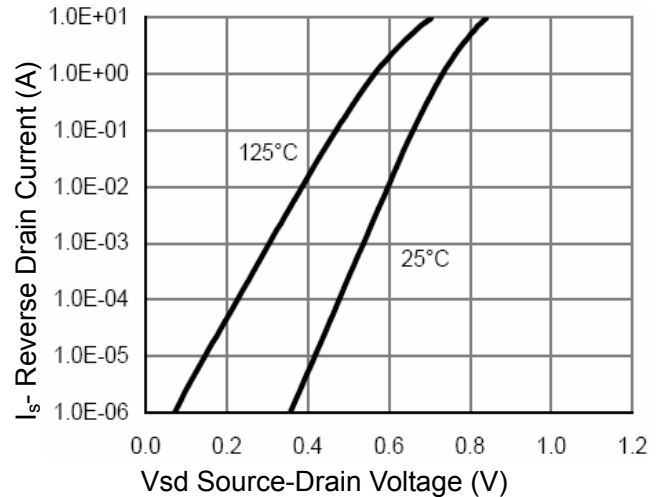
**Figure 3 Rdson- Drain Current**



**Figure 4 Rdson-Junction Temperature**



**Figure 5 Gate Charge**



**Figure 6 Source- Drain Diode Forward**

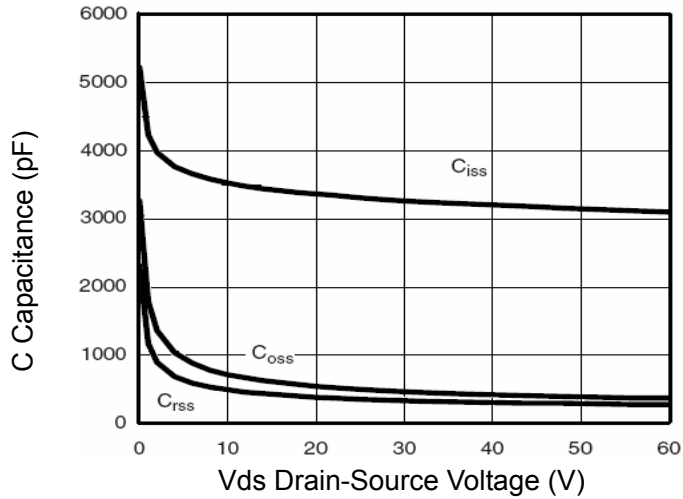


Figure 7 Capacitance vs Vds

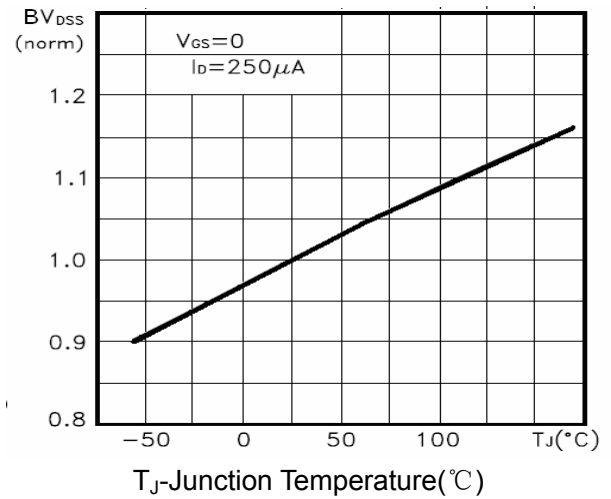


Figure 9 BV<sub>DSS</sub> vs Junction Temperature

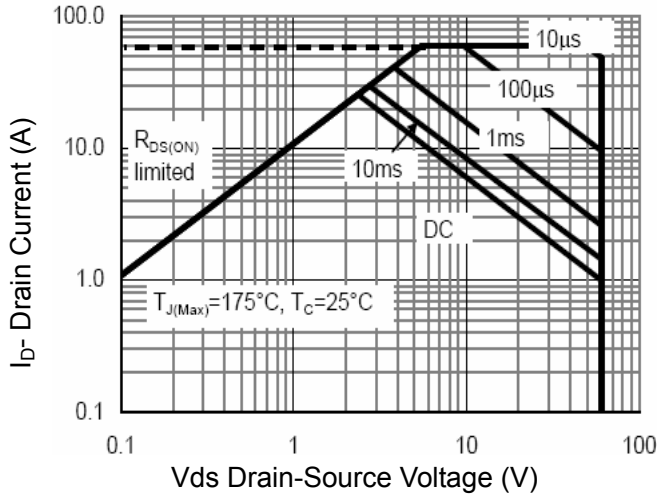


Figure 8 Safe Operation Area

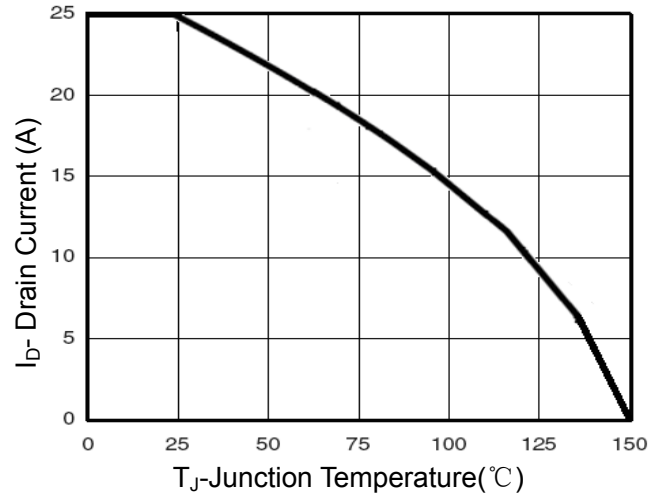


Figure 10 ID Current De-rating

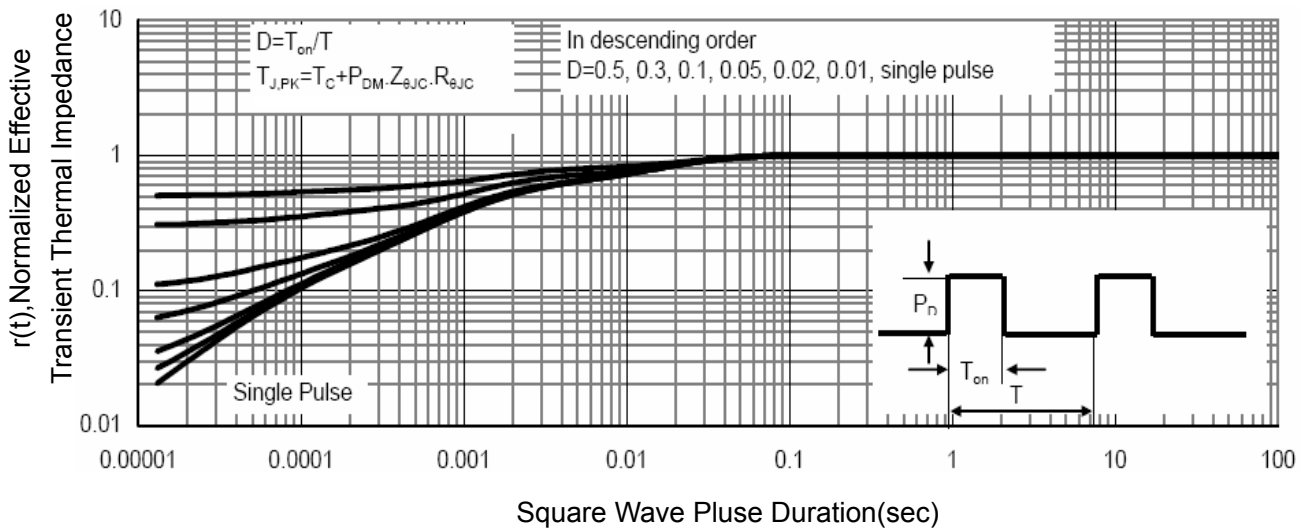
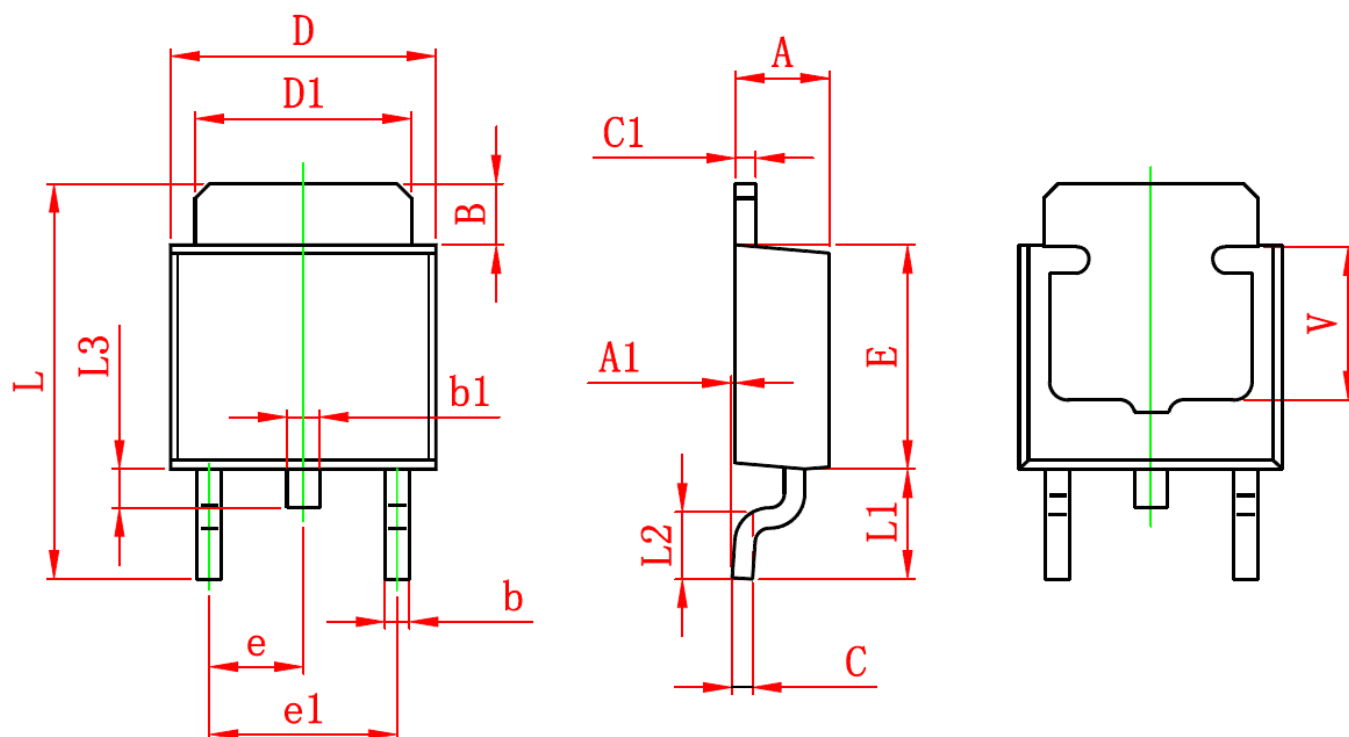


Figure 11 Normalized Maximum Transient Thermal Impedance

**TO-252-2L PACKAGE OUTLINE DIMENSIONS**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP.		0.091 TYP.	
e1	4.500	4.700	0.177	0.185
L	9.500	9.900	0.374	0.390
L1	2.550	2.900	0.100	0.114
L2	1.400	1.780	0.055	0.070
L3	0.600	0.900	0.024	0.035
V	3.800 REF.		0.150 REF.	

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