

## P-Channel Enhancement Mode Power MOSFET

### Description

The HM25P15K uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

### General Features

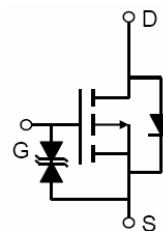
- $V_{DS} = -150V, I_D = -25A$   
 $R_{DS(ON)} < 135m\Omega @ V_{GS} = -10V$  (Typ. = 120mR)  
 $R_{DS(ON)} < 160m\Omega @ V_{GS} = -4.5V$  (Typ. = 131mR)
- Super high dense cell design
- Advanced trench process technology
- Reliable and rugged
- High density cell design for ultra low On-Resistance

### Application

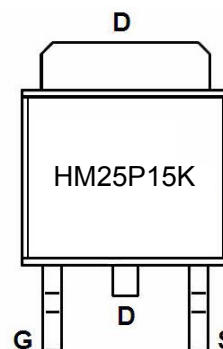
- Portable equipment and battery powered systems

**100% UIS TESTED!**

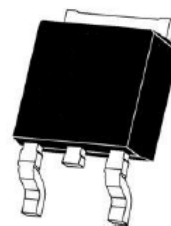
**100%  $\Delta V_{ds}$  TESTED!**



Schematic diagram



Marking and pin assignment



TO-252-2L top view

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM25P15K	HM25P15K	TO-252-2L	Ø330mm	12mm	2500 units

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-150	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	-25	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D (100^\circ C)$	-17	A
Pulsed Drain Current	$I_{DM}$	-140	A
Maximum Power Dissipation	$P_D$	160	W
Derating factor		1.3	W/ $^\circ C$
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ C$

## Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta jc}$	0.8	$^{\circ}\text{C/W}$
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## Electrical Characteristics ( $T_C=25^{\circ}\text{C}$ unless otherwise noted)

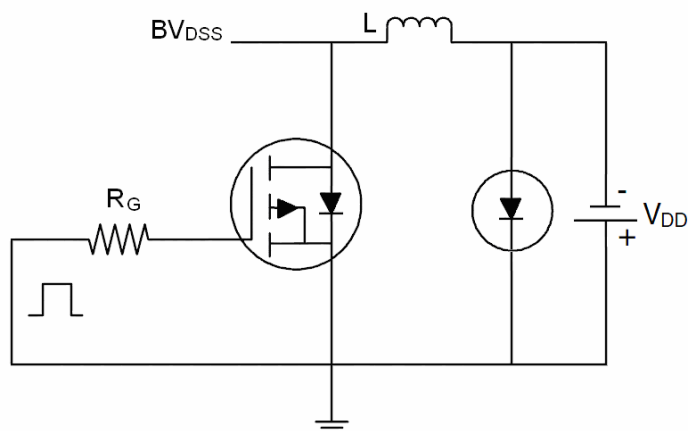
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =-250μA	-145	-155	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-145V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±10	μA
On Characteristics <sup>(Note 3)</sup>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.5	-1.9	-3	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-20A	-	120	135	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-20A	-	131	160	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =-5V, I <sub>D</sub> =-20A	5	-	-	S
Dynamic Characteristics <sup>(Note4)</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-75V, V <sub>GS</sub> =0V, F=1.0MHz	-	7650	-	PF
Output Capacitance	C <sub>oss</sub>		-	148	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	131	-	PF
Switching Characteristics <sup>(Note 4)</sup>						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =-75V, I <sub>D</sub> =-20A V <sub>GS</sub> =-10V, R <sub>GEN</sub> =9.1Ω	-	17	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	80	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	45	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	65	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-75V, I <sub>D</sub> =-20A, V <sub>GS</sub> =-10V	-	137	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	25	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	28	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <sup>(Note 3)</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =-25A	-	-	-1.2	V
Diode Forward Current <sup>(Note 2)</sup>	I <sub>S</sub>	-	-	-	-25	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25°C, I <sub>F</sub> =-25A di/dt = 100A/μs <sup>(Note3)</sup>	-	90	-	nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	105	-	nC

## Notes:

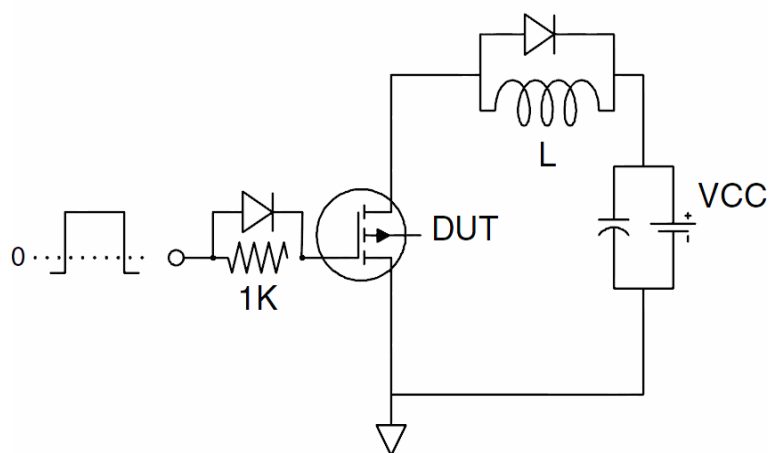
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition:  $T_J=25^{\circ}\text{C}, V_{DD}=-75V, V_G=-10V, L=0.5mH, R_g=25\Omega$

## Test Circuit

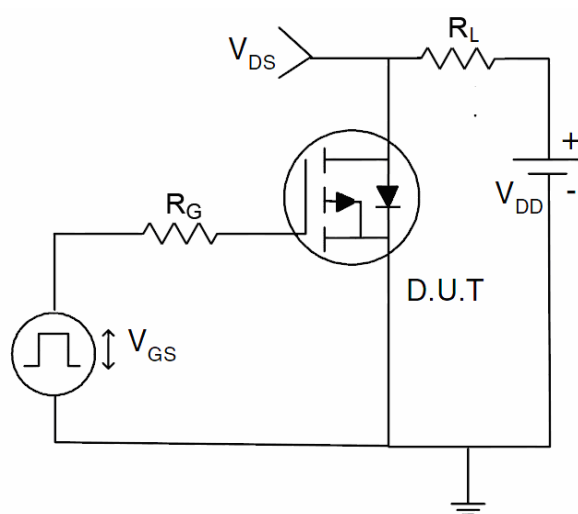
### 1) $E_{AS}$ Test Circuit



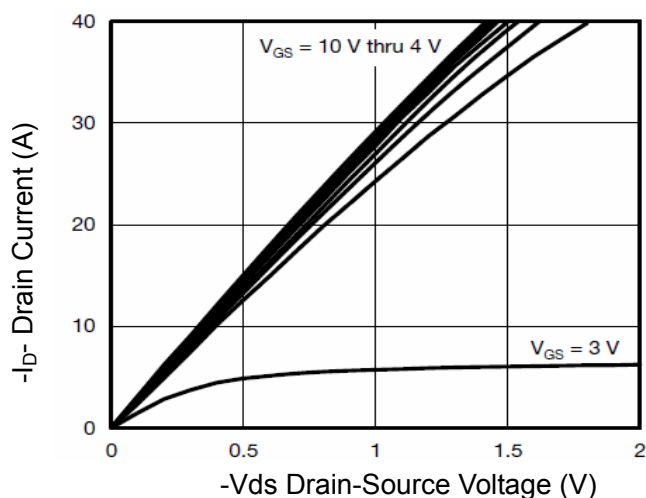
### 2) Gate Charge Test Circuit



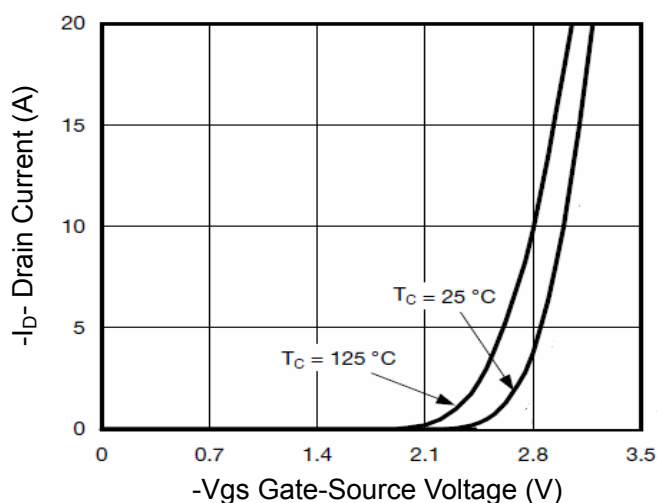
### 3) Switch Time Test Circuit



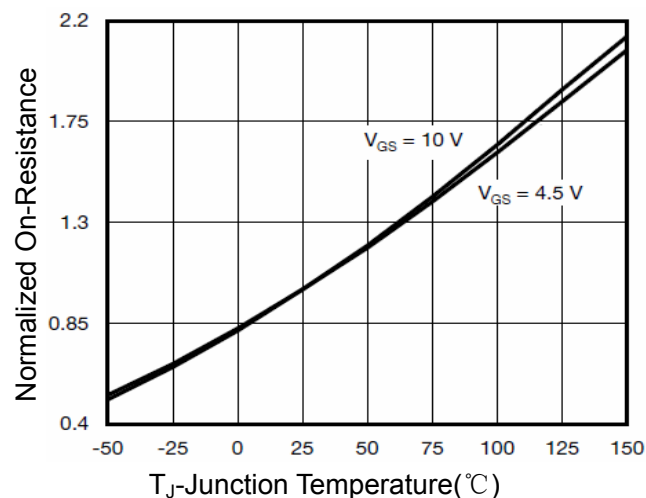
## Typical Electrical and Thermal Characteristics (Curves)



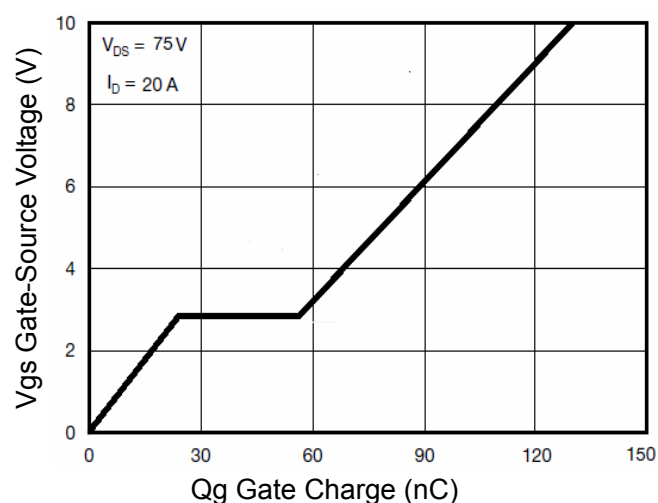
**Figure 1 Output Characteristics**



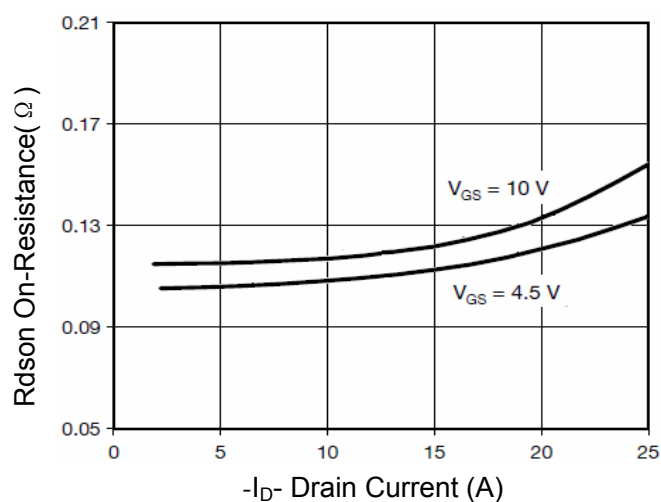
**Figure 2 Transfer Characteristics**



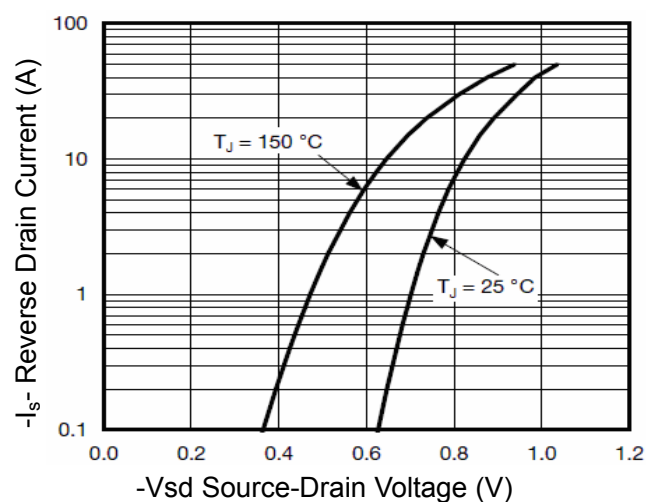
**Figure 4  $R_{DS(on)}$ -Junction Temperature**



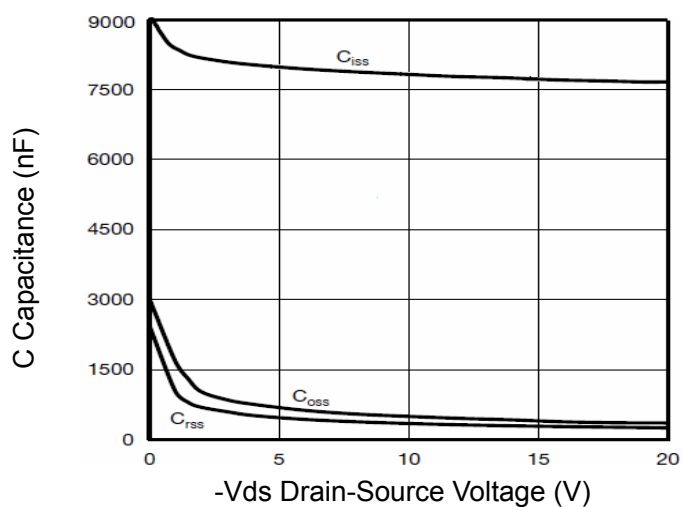
**Figure 5 Gate Charge**



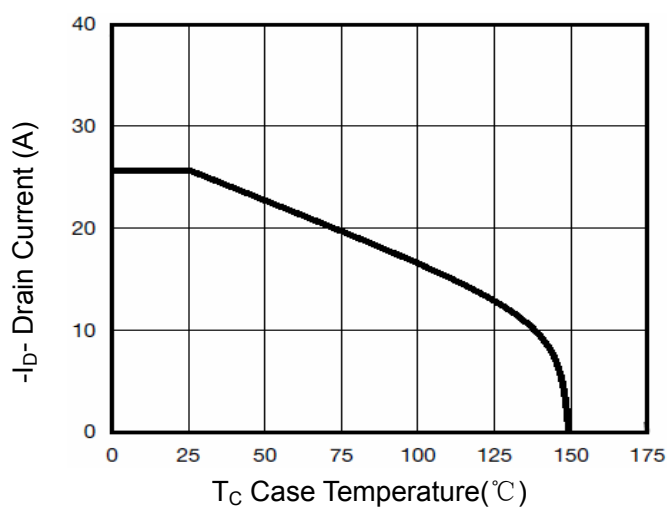
**Figure 3  $R_{DS(on)}$ - Drain Current**



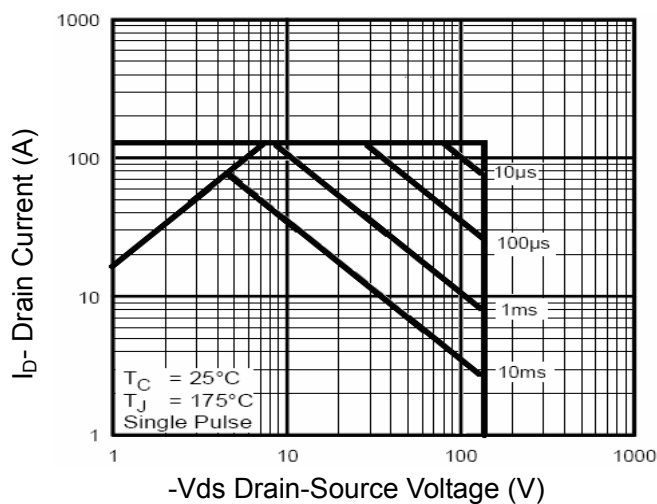
**Figure 6 Source- Drain Diode Forward**



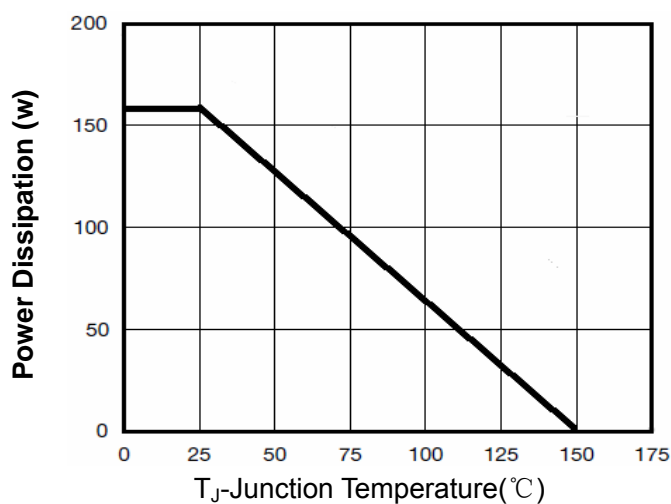
**Figure 7 Capacitance vs Vds**



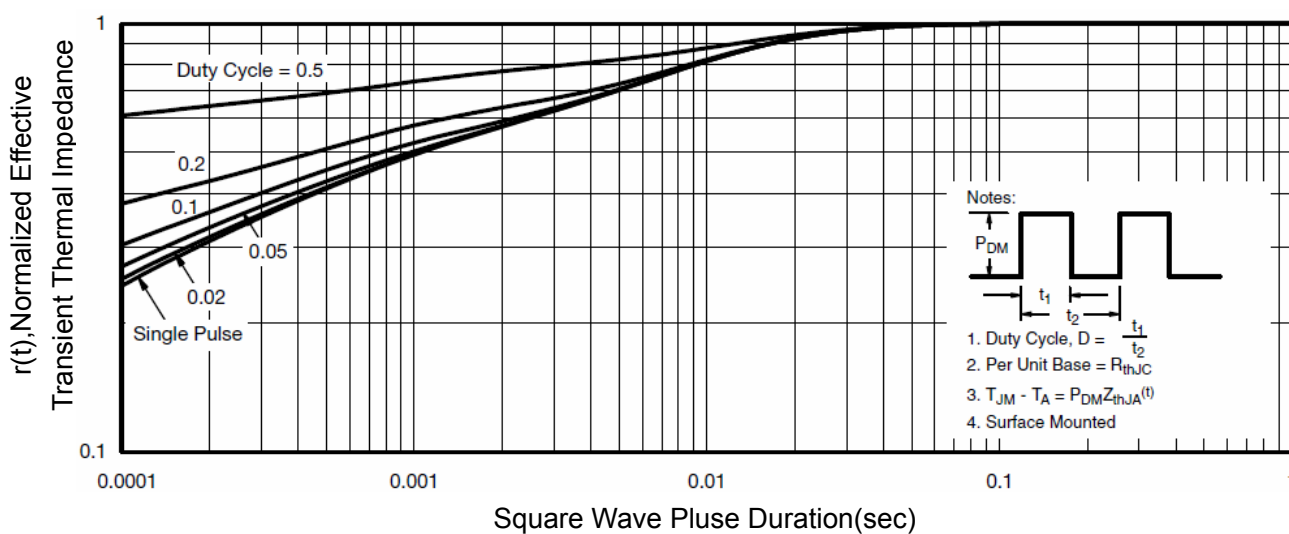
**Figure 9 Drain Current vs Case Temperature**



**Figure 8 Safe Operation Area**

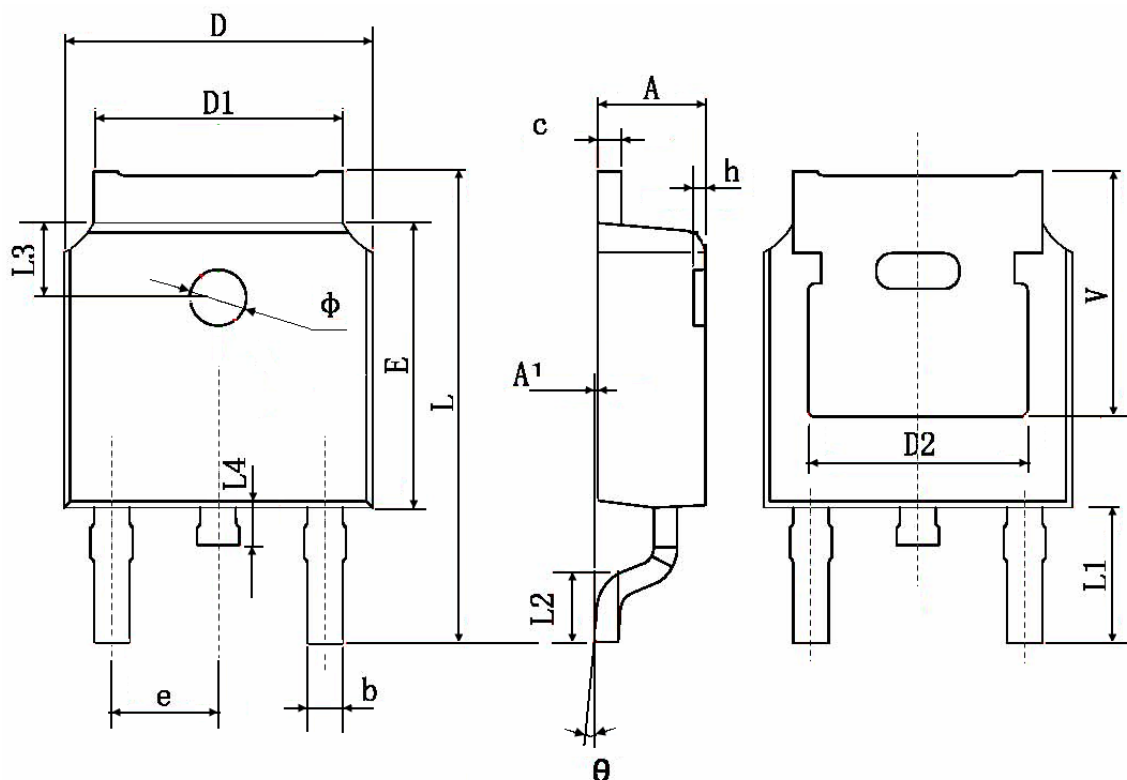


**Figure 10 Power De-rating**



**Figure 11 Normalized Maximum Transient Thermal Impedance**

## TO-252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.83 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

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