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## Dual Channel 700mA Synchronous Buck DC/DC Converter

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### Features

- Current mode operation for excellent line and load transient response
- Low quiescent current: 70 $\mu$ A
- 700mA Output Current
- 2.5V to 5.5V Input Voltage Range
- No Schottky Diode Required
- Output voltage: 0.6V~5.5V
- 1.4MHz fixed frequency switching
- Short-Circuit protection
- Low profile SOT-23-6L package (lead-free packaging is now available)

### Applications

- Digital cameras and MP3
- Palmtop computers / PDAs
- Cellular phones
- Wireless handsets and DSL modems
- Portable media players
- PC cards

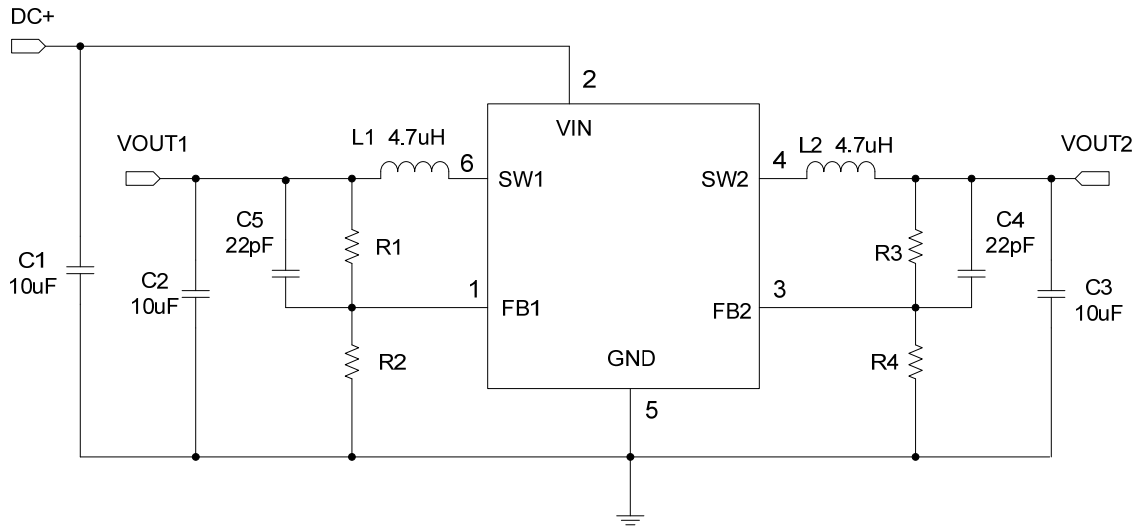
### Description

The PTH1FG is a high efficiency synchronous, dual channel 700mA Synchronous Buck DC/DC converter working under an input voltage range of 2.5V to 5.5V. It integrates two synchronous buck DC-DC converters. 100% duty cycle capability extends battery life in portable devices, while the quiescent current is 70 $\mu$ A with no load.

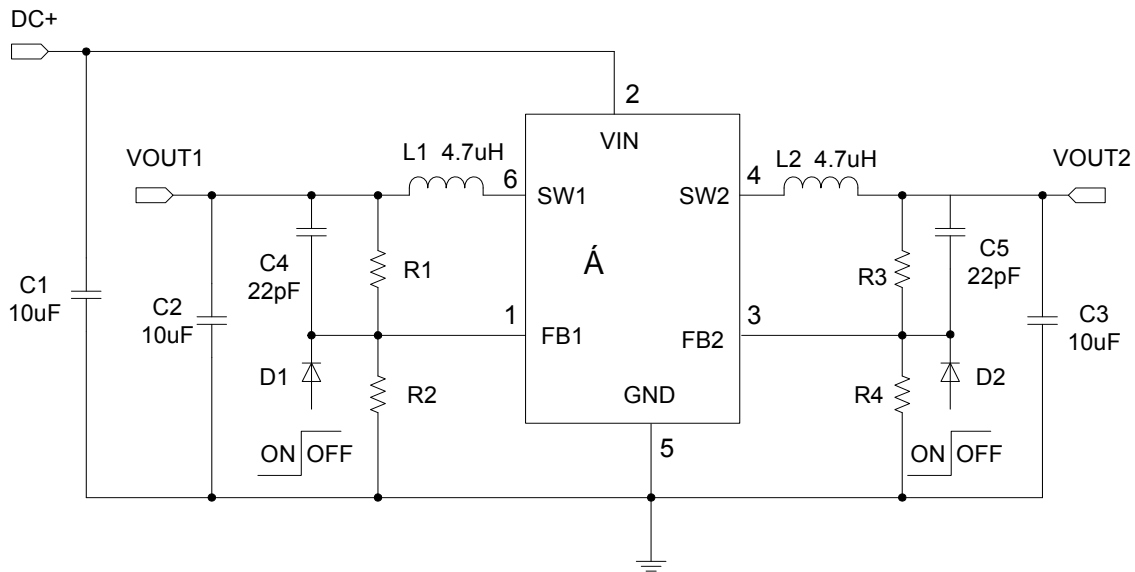
Switching frequency is internally set at 1.4MHz, allowing the use of small surface mount inductors and capacitors.

The PTH1FG converters are available in the industry standard SOT-23-6L packages (or upon request).

Typical Application Circuits



\* Adjustable Output Voltage:  $V_{OUT1} = 0.6V \cdot [1 + (R1/R2)]$ ,  $V_{OUT2} = 0.6V \cdot [1 + (R3/R4)]$ .



\* ON/OFF Control: Connecting the positive end of D1 to GND enables the VOUT1, connecting the positive end of D2 to GND enables the VOUT2. Connecting the positive end of D1 to VIN shuts down the VOUT1, connecting the positive end of D2 to VIN shuts down the VOUT2.

## Pin Assignment and Description

TOP VIEW		PIN	NAME	DESCRIPTION
		1	FB1	Feedback Sense for VOUT1
		2	VIN	Input
		3	FB2	Feedback Sense for VOUT2
		4	SW2	Switch Node for VOUT2
		5	GND	Ground
		6	SW1	Switch Node for VOUT1

## Absolute Maximum Ratings (Note 1)

- Input Supply Voltage ..... – 0.3V to 8V
- FB1, FB2 Voltages ..... – 0.3V to VIN
- SW1, SW2 Voltages ..... - 0.3 V ~ (VIN + 0.3) V
- Peak SW1, SW2 Sink and Source Current.....1.3A
- Operating Temperature Range (Note 2).....- 40°C ~ + 85°C
- Lead Temperature (Soldering 10 sec.) .....265°C
- Storage Temperature Range .....- 65°C ~ + 150°C
- Junction Temperature (Note 3).....150°C

**Note 1.** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** The PTH FGs guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

**Note 3:** TJ is calculated from the ambient temperature TA and power dissipation PD according to the following formula:

$$P_{TH\ FG} T_J = T_A + (PD)(280^{\circ}C/W)$$

## Electrical Characteristics

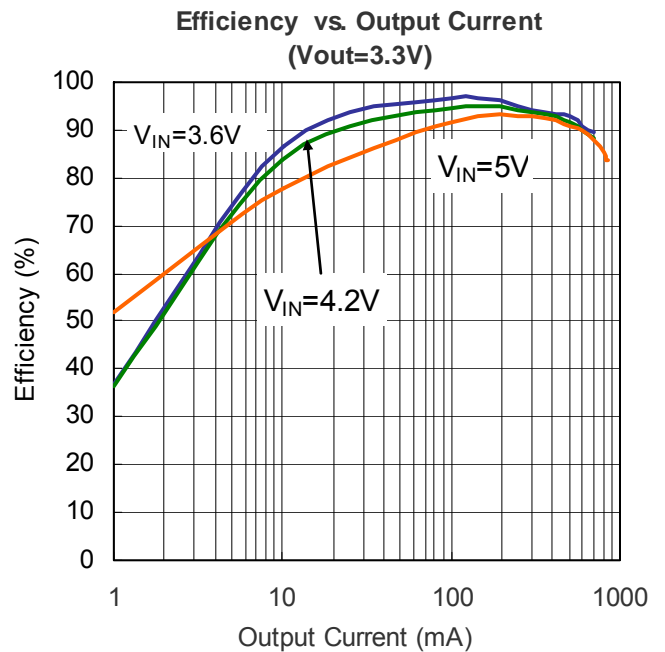
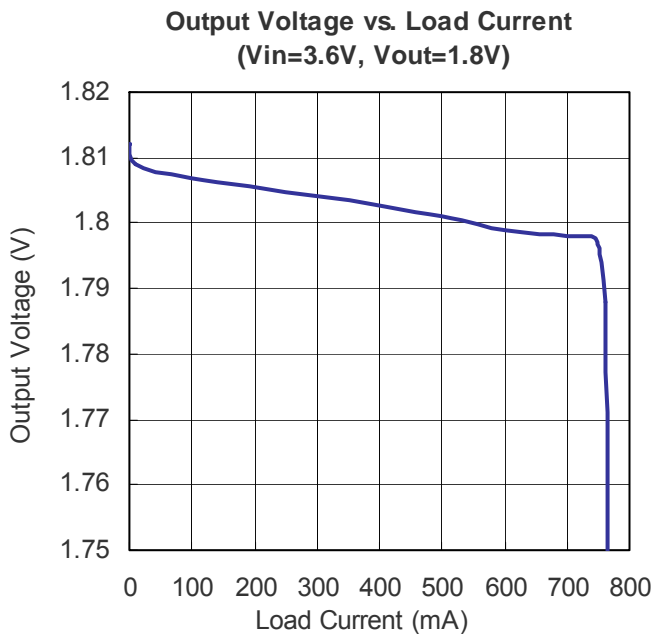
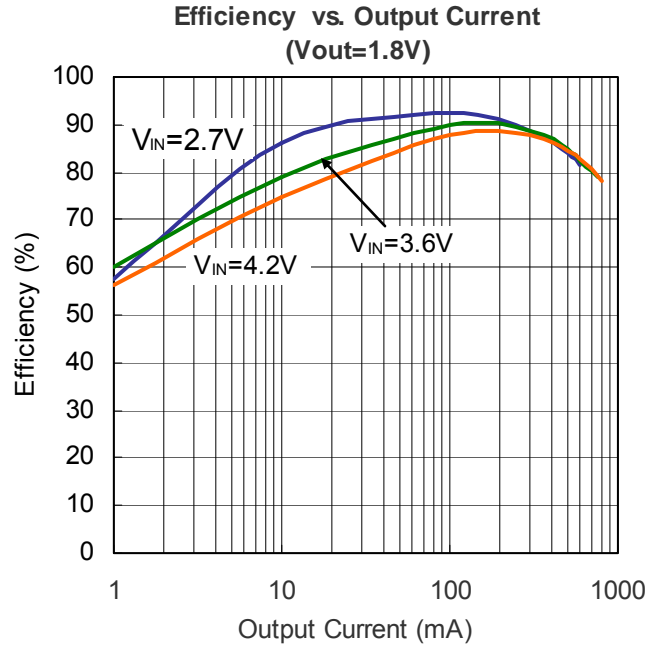
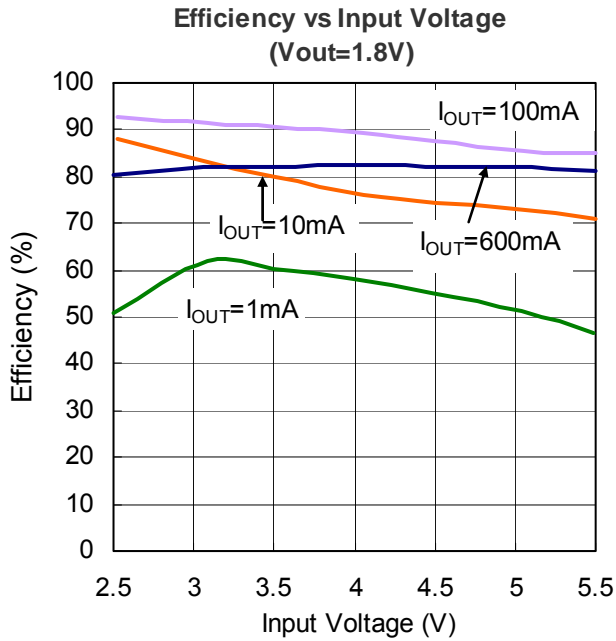
Operating Conditions: TA = 25°C, R1=R3=200k, R2=R4=100k, C1 =10μF, C2=C3 = 10μF, C4=C5 = 22pF, L1=L2=4.7uH, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V <sub>OUT1,2</sub>	Output Voltage		0.6		5.5	V
V <sub>IN</sub>	Input Voltage Range		2.5		5.5	V
V <sub>FB1,2</sub>	Regulated Voltage		0.583	0.6	0.617	V
ΔV <sub>FB1,2</sub>	V <sub>REF</sub>	V <sub>IN</sub> =2.5V~5.5V		0.4		%/V
F <sub>OSC1,2</sub>	Oscillator Frequency	I <sub>LOAD</sub> = 100mA		1.4		MHz
I <sub>Q</sub>	Quiescent Current	I <sub>LOAD</sub> = 0A		70		μA
I <sub>PK1,2</sub>	Peak Inductor Current	V <sub>IN</sub> = 3V, or V <sub>OUT</sub> = 90%, Duty Cycle < 35%		0.9		A
R <sub>PFET</sub>	R <sub>DS(ON)</sub> of P-Channel FET	V <sub>IN</sub> =3.6V, I <sub>OUT1,2</sub> = 700mA		0.3		Ω
R <sub>NFET</sub>	R <sub>DS(ON)</sub> of N-Channel FET	V <sub>IN</sub> =3.6V, I <sub>OUT1,2</sub> = -700mA		0.57		Ω
ΔV <sub>OUT</sub>	V <sub>OUT1,2</sub> Line Regulation	V <sub>IN</sub> =2.5V~5.5V		0.4		%/V
V <sub>LOADREG</sub>	V <sub>OUT1,2</sub> Load Regulation			1		%

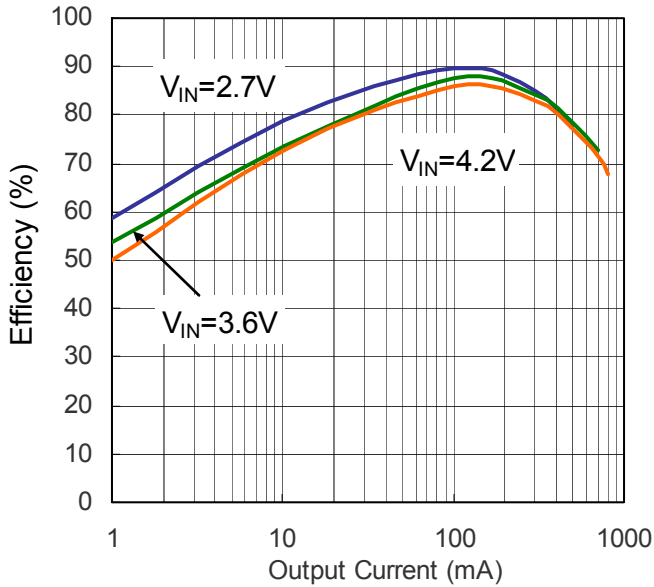
## Typical Operating Characteristics

Operating Conditions: TA = 25°C, C1 = 10µF, C2=C3 = 10µF, C4=C5 = 22pF, L1=L2=4.7µH, unless otherwise specified.

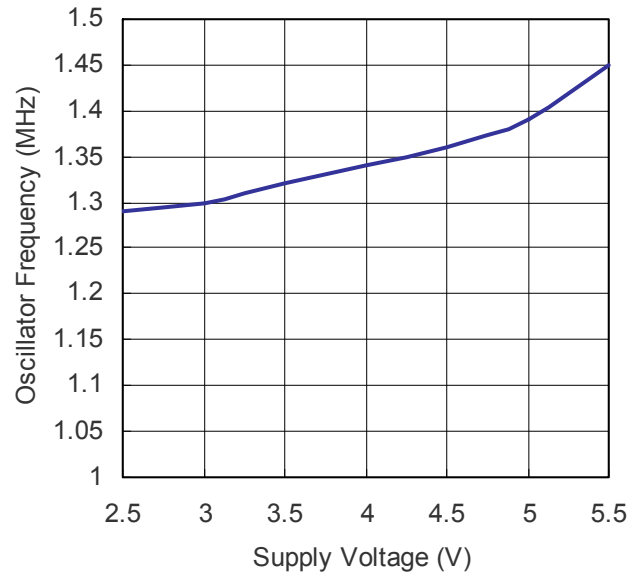
VOUT1 or VOUT2:



**Efficiency vs. Output Current**  
 (Vout=1.2V)

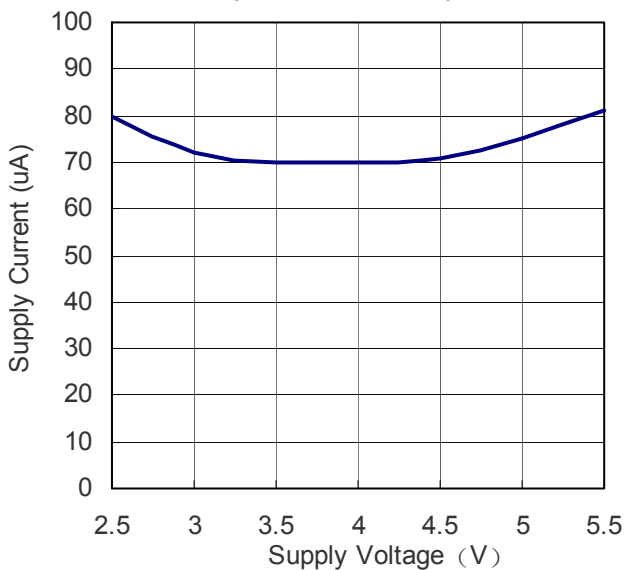


**Oscillator Frequency vs. Supply Voltage**  
 (Vout=1.8V Io=100mA)

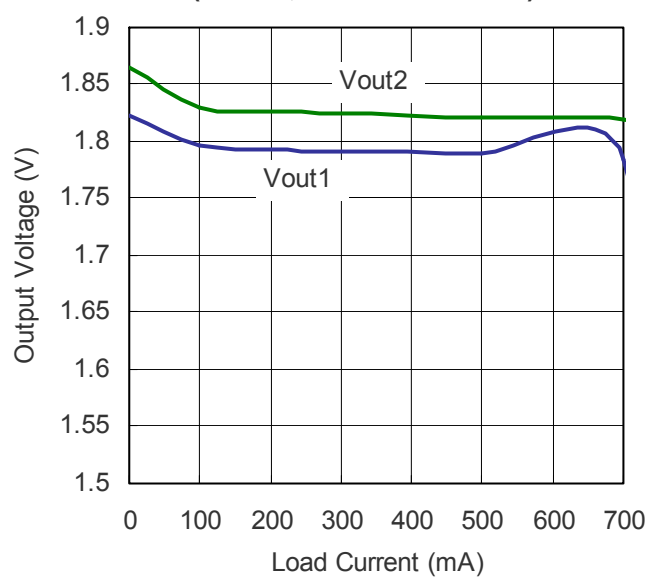


**VOUT1 and VOUT2**

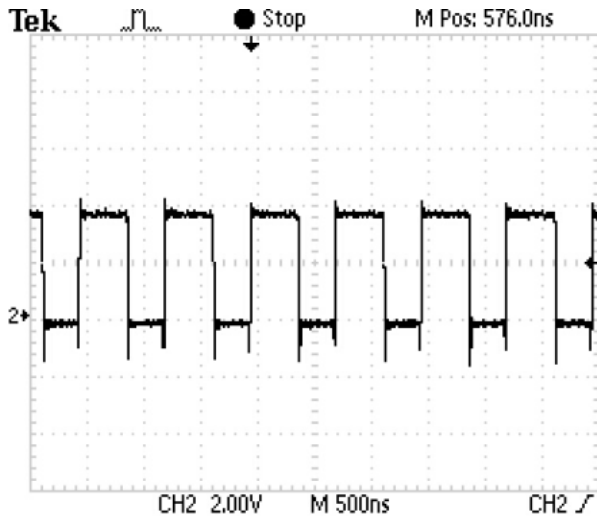
**Supply Current vs. Supply Voltage**  
 (Vout=1.8V Io=0A)



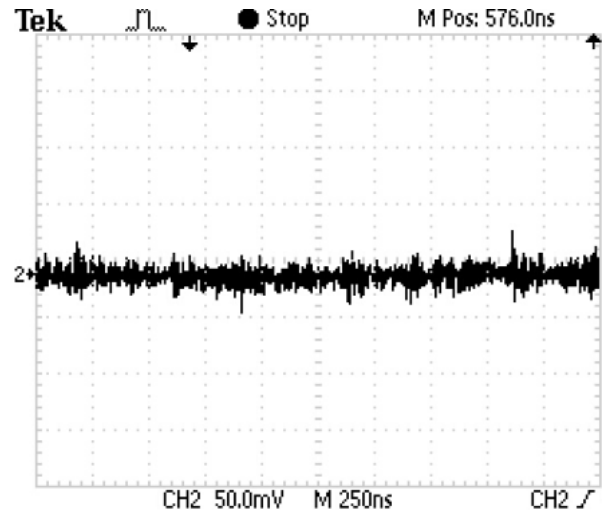
**Output Voltage vs. Load Current**  
 (Vin=5V, Vout1=Vout2=1.8V)



**SW Ripple**  
(VIN=3.6V IOUT=100m A VOUT=1.8V)



**Output Ripple**  
(VIN=3.6V IOUT=100m A VOUT=1.8V)



## Pin Functions

**FB1 (Pin 1):** Feedback Sense for VOUT1. Receive the feedback voltage from an external resistive divider across the output 1. The output voltage is set by a resistive divider according to the following formula:  $V_{OUT1} = 0.6V \cdot [1 + (R1/R2)]$ .

**VIN (Pin 2):** Power Supply Pin. It must be closely decoupled to GND, and with a 10μF or greater ceramic capacitor.

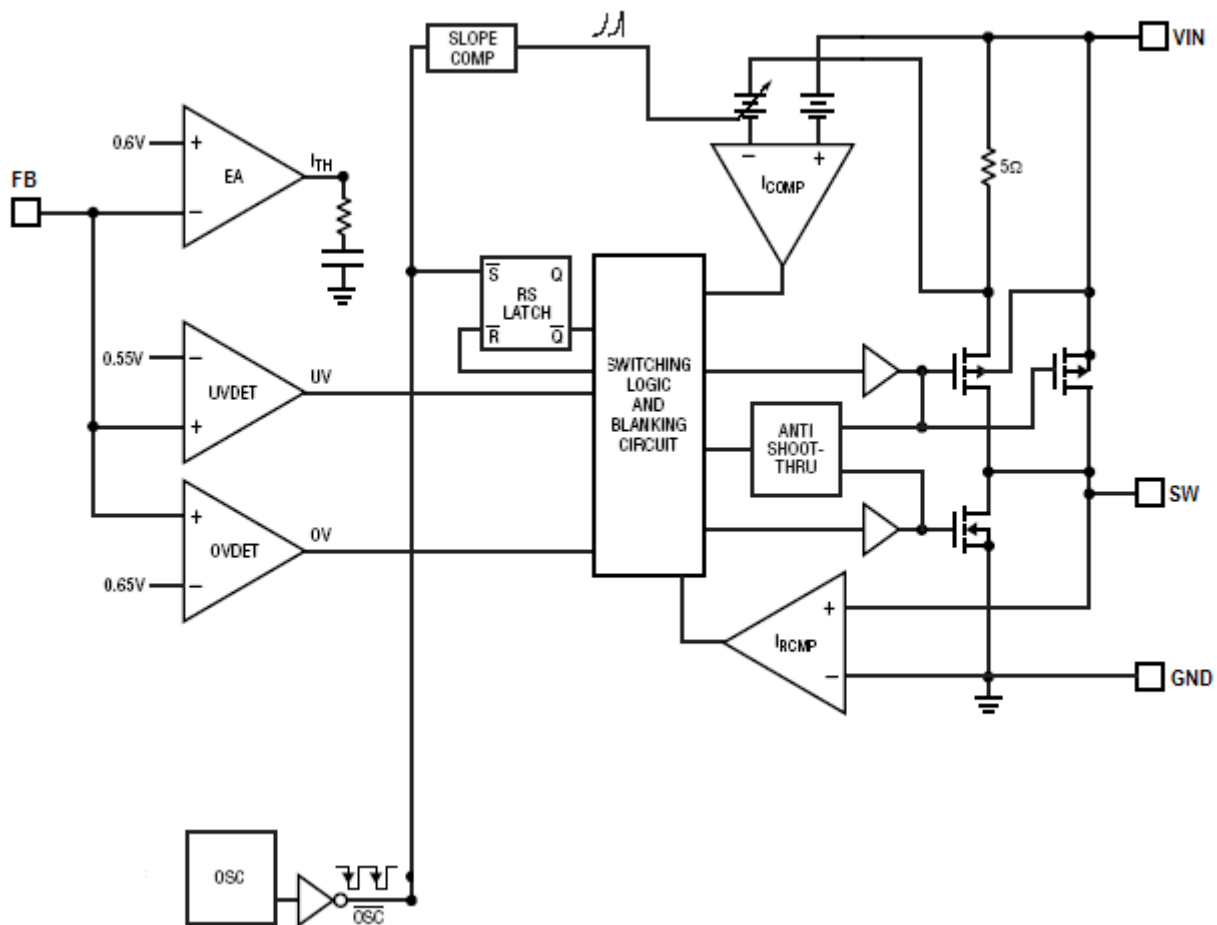
**FB2 (Pin 3):** Feedback Sense for VOUT2. Receive the feedback voltage from the external resistive divider across the output. The output voltage is set by a resistive divider according to the following formula:  $V_{OUT2} = 0.6V \cdot [1 + (R3/R4)]$ .

**SW2 (Pin 4):** Switch Node for VOUT2. This pin connects to the drains of the internal main and synchronous power MOSFET switches.

**GND (Pin 5):** Ground Pin.

**SW1 (Pin 6):** Switch Node for VOUT1. This pin connects to the drains of the internal main and synchronous power MOSFET switches.

## Block Diagram





## Application Information

The basic PTH FG application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by CIN and COUT.

### Inductor Selection

For most applications, the value of the inductor will fall in the range of 1μH to 4.7μH. Its value is chosen based on the desired ripple current. Large value inductors lower ripple current and small value inductors result in higher ripple currents. Higher VIN or VOUT also increases the ripple current as shown in equation. A reasonable starting point for setting ripple current is  $\Delta I_L = 280\text{mA}$  (40% of 700mA).

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT} \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 840mA rated inductor should be enough for most applications (700mA + 140mA). For better efficiency, choose a low DC-resistance inductor.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or perm alloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs. size requirements and any radiated field/EMI requirements than on what the PTH FG requires to operate.

### Output and Input Capacitor Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle  $V_{OUT}/V_{IN}$ . To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ required } I_{RMS} \cong I_{O\text{MAX}} \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{1/2}}{V_{IN}}$$

This formula has a maximum at  $V_{IN} = 2V_{OUT}$ , where  $I_{RMS} = I_{OUT}/2$ . This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

The selection of  $C_{OUT}$  is driven by the required effective series resistance (ESR). Typically, once the ESR requirement for  $C_{OUT}$  has been met, the RMS current rating generally far exceeds the  $I_{RIPPLE(P-P)}$  requirement. The output ripple  $\Delta V_{OUT}$  is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left( \text{ESR} + \frac{1}{8fC_{OUT}} \right)$$

Where  $f$  = operating frequency,  $C_{OUT}$  = output capacitance and  $\Delta I_L$  = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since  $\Delta I_L$  increases with input voltage.

Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum. These are specially constructed and tested for low ESR so they give the lowest ESR for a given volume. Other capacitor types include Sanyo POSCAP, Kemet T510 and T495 series, and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

### Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as: Efficiency = 100% - (L1+ L2+ L3+ ...) where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: VIN quiescent current and  $I^2R$  losses. The VIN quiescent current loss dominates the efficiency loss at very low load currents whereas the  $I^2R$  loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The VIN quiescent current is due to two components: the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge  $\Delta Q$  moves from VIN to ground. The resulting  $\Delta Q/\Delta t$  is the current out of VIN that is typically larger than the DC bias current. In continuous mode,  $I_{GATECHG} = f(Q_T + Q_B)$  where  $Q_T$  and  $Q_B$  are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to VIN and thus their effects will be more pronounced at higher supply voltages.

2.  $I^2R$  losses are calculated from the resistances of the internal switches,  $R_{SW}$  and external inductor  $R_L$ . In continuous mode the average output current flowing through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET  $R_{DS(ON)}$  and the duty cycle (DC) as follows:  $R_{SW} = R_{DS(ON)TOP} \times DC + R_{DS(ON)BOT} \times (1-DC)$  The  $R_{DS(ON)}$  for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain  $I^2R$  losses, simply add  $R_{SW}$  to  $R_L$  and multiply the result by the square of the average output current. Other losses including CIN and COUT ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

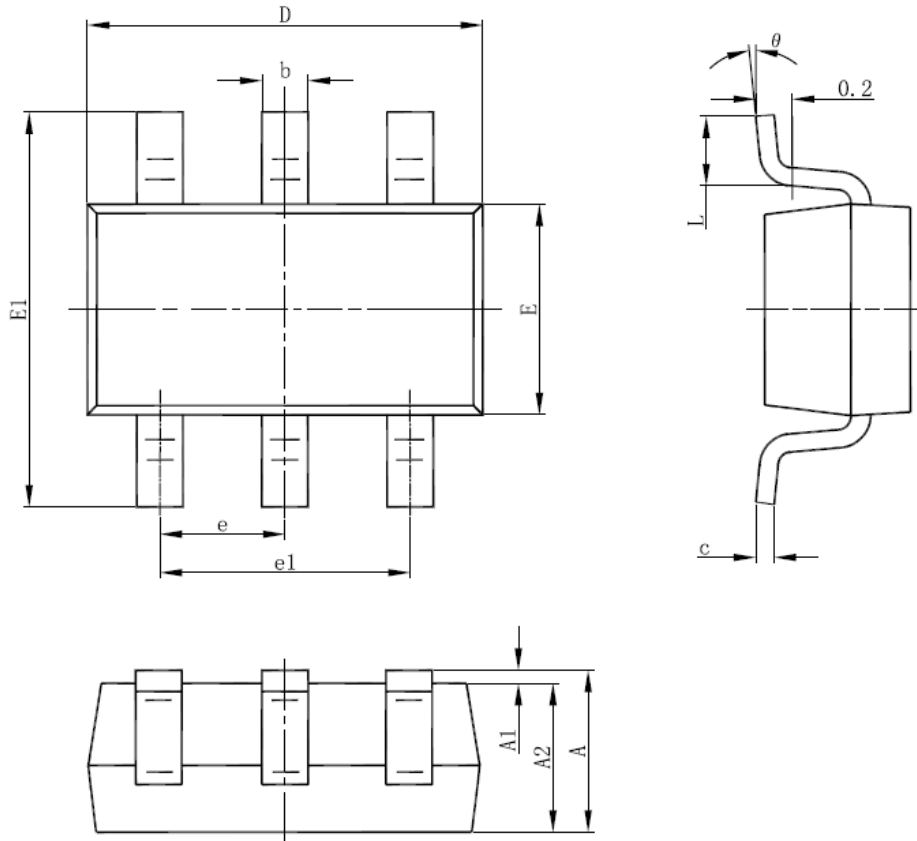
### PCB Layout Guidelines

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the PTH FG Check the following in your layout:

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1. The power traces, consisting of the GND trace, the SW1,SW2 trace and the VIN trace should be kept short, direct and wide.
  2. Put the input capacitor as close as possible to the device pins (VIN and GND).
  3. SW1, SW2 node is with high frequency voltage swing and should be kept small area. Keep analog components away from SW1, SW2 node to prevent stray capacitive noise pick-up.
  4. Connect all analog grounds to a common node and then connect the common node to the power ground behind the output capacitors.

## Packaging Information

SOT-23-6L Surface Mount Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°