P-Channel Enhancement Mode Power MOSFET

Description

The HM35P04D uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge .This device is well suited for high current load applications.

General Features

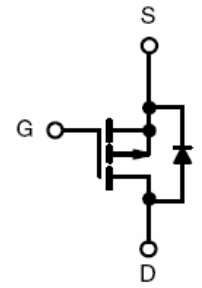
- V_{DS} =-40V,I_D =-35A
  $R_{DS(ON)}$ <10mΩ @ V_{GS}=-10V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

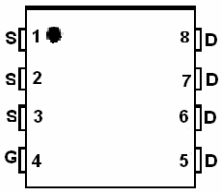
- Power switch
- Load switch in high current applications
- DC/DC converters

100% UIS TESTED!

100% ΔVds TESTED!



Schematic diagram



Marking and pin assignment

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM35P04D	HM35P04D	DFN5X6-8L	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	-35	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	-25	A
Pulsed Drain Current	I_{DM}	-105	A
Maximum Power Dissipation	P_D	65	W
Derating factor		0.52	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	1020	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance, Junction-to-Case(Note 2)	$R_{\theta JC}$	1.92	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

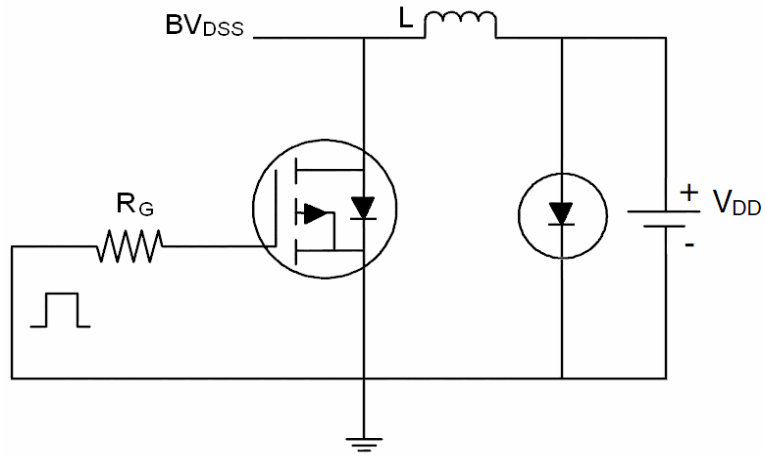
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-40V,V_{GS}=0V	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-1.2	-1.9	-2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-20A	-	7.5	10	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-10V,I_D=-20A	-	50	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=-20V,V_{GS}=0V, F=1.0MHz	-	6460	-	PF
Output Capacitance	C_{oss}		-	684	-	PF
Reverse Transfer Capacitance	C_{rss}		-	600	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-20V, R_L=2Ω, V_{GS}=-10V,R_G=1Ω	-	15	-	nS
Turn-on Rise Time	t_r		-	12	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	35	-	nS
Turn-Off Fall Time	t_f		-	18	-	nS
Total Gate Charge	Q_g	V_{DS}=-20,I_D=-20A, V_{GS}=-10V	-	106		nC
Gate-Source Charge	Q_{gs}		-	22		nC
Gate-Drain Charge	Q_{gd}		-	27		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=-10A	-		-1.2	V
Diode Forward Current (Note 2)	I_S		-	-	-35	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF =- 10A di/dt = -100A/μs(Note3)	-	53		nS
Reverse Recovery Charge	Qrr		-	50		nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

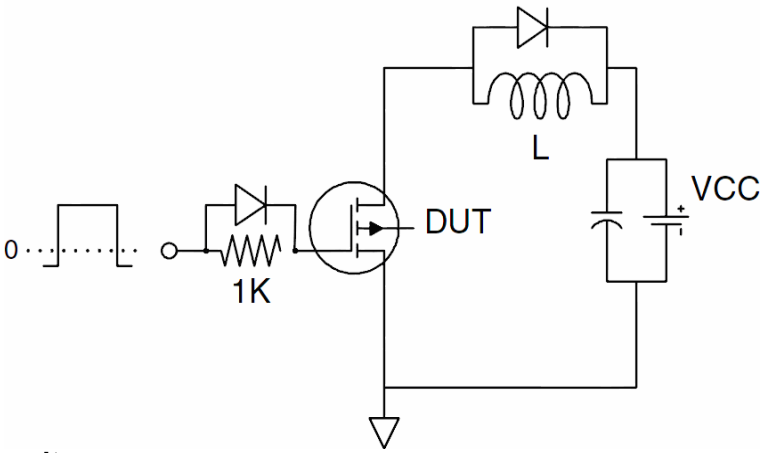
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. E_{AS} condition: Tj=25℃,V_{DD}=-20V,V_G=-10V,L=1mH,Rg=25Ω,I_{AS}=45A

Test Circuit

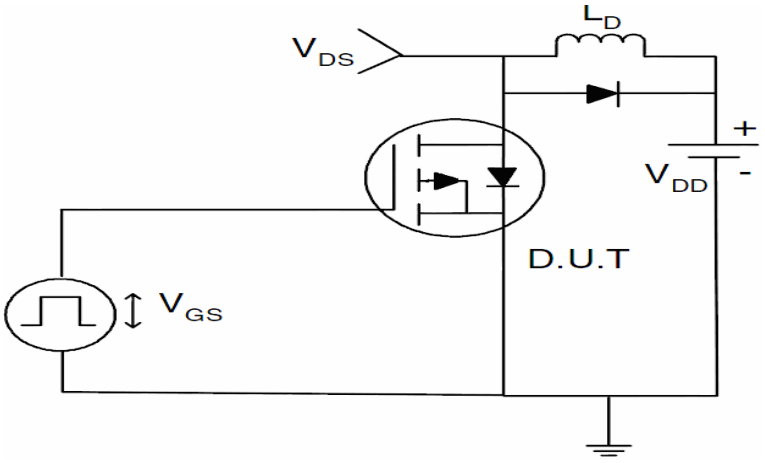
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

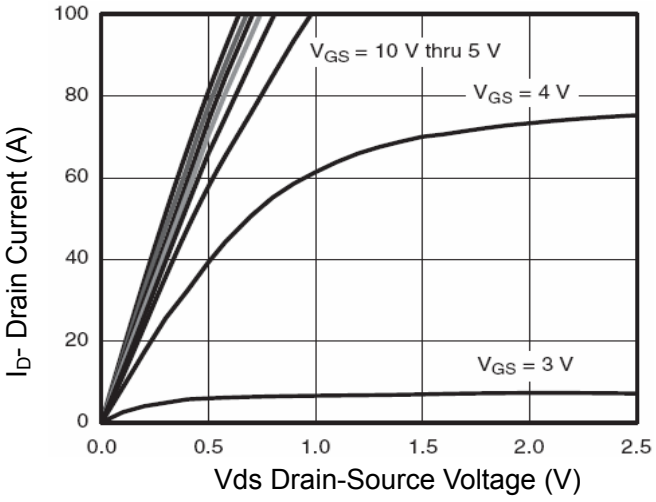


Figure 1 Output Characteristics

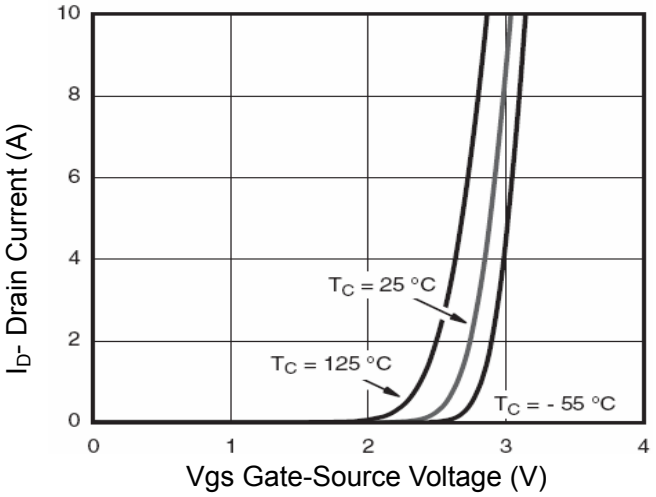


Figure 2 Transfer Characteristics

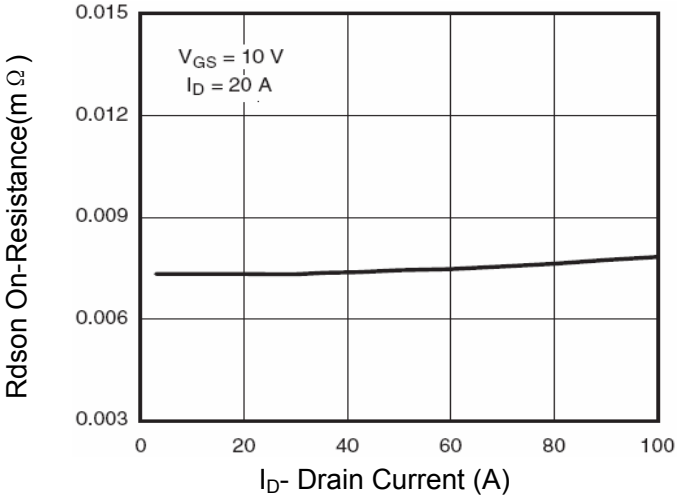


Figure 3 Rdson- Drain Current

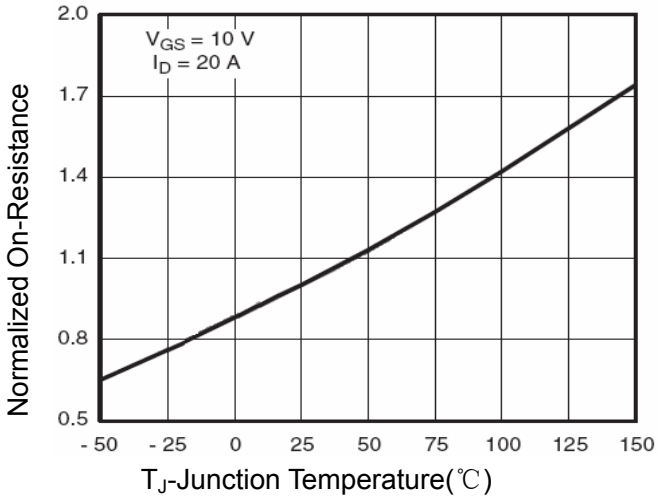


Figure 4 Rdson-Junction Temperature

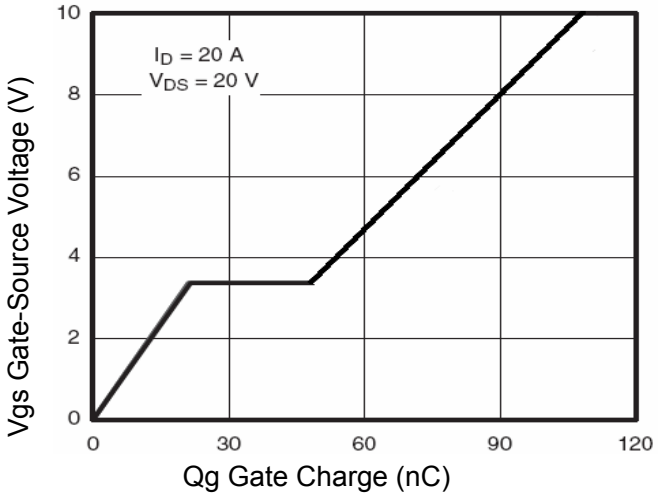


Figure 5 Gate Charge

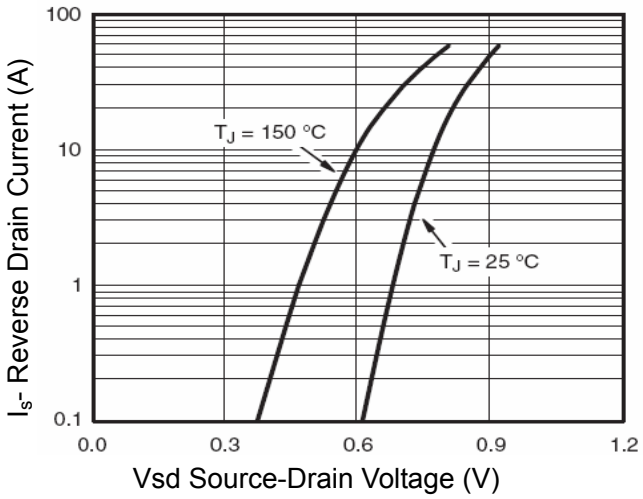


Figure 6 Source- Drain Diode Forward

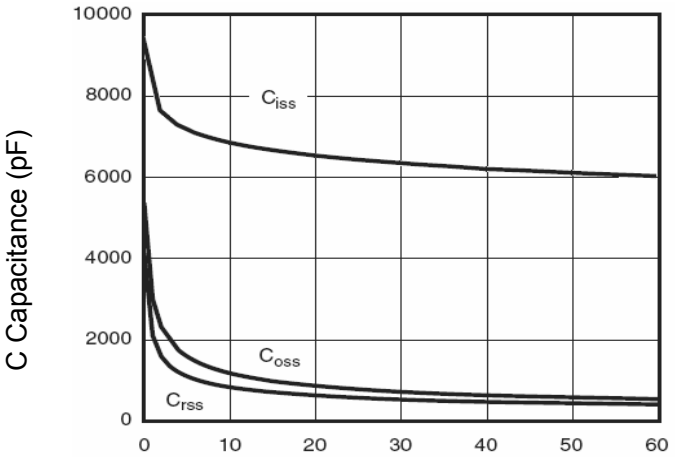


Figure 7 Capacitance vs Vds

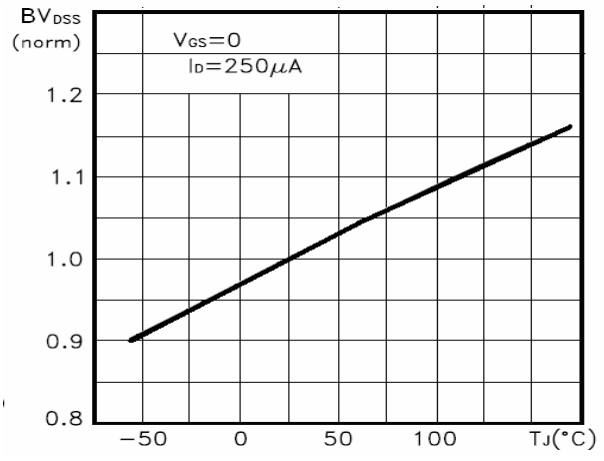


Figure 9 BV_{DSS} vs Junction Temperature

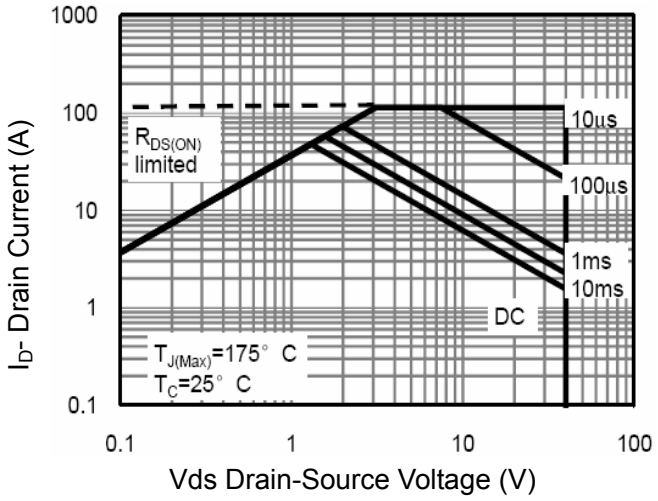


Figure 8 Safe Operation Area

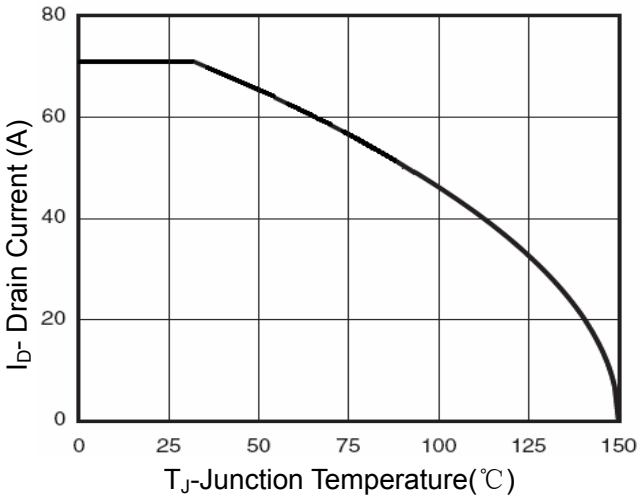


Figure 10 ID Current Derating vs Junction Temperature

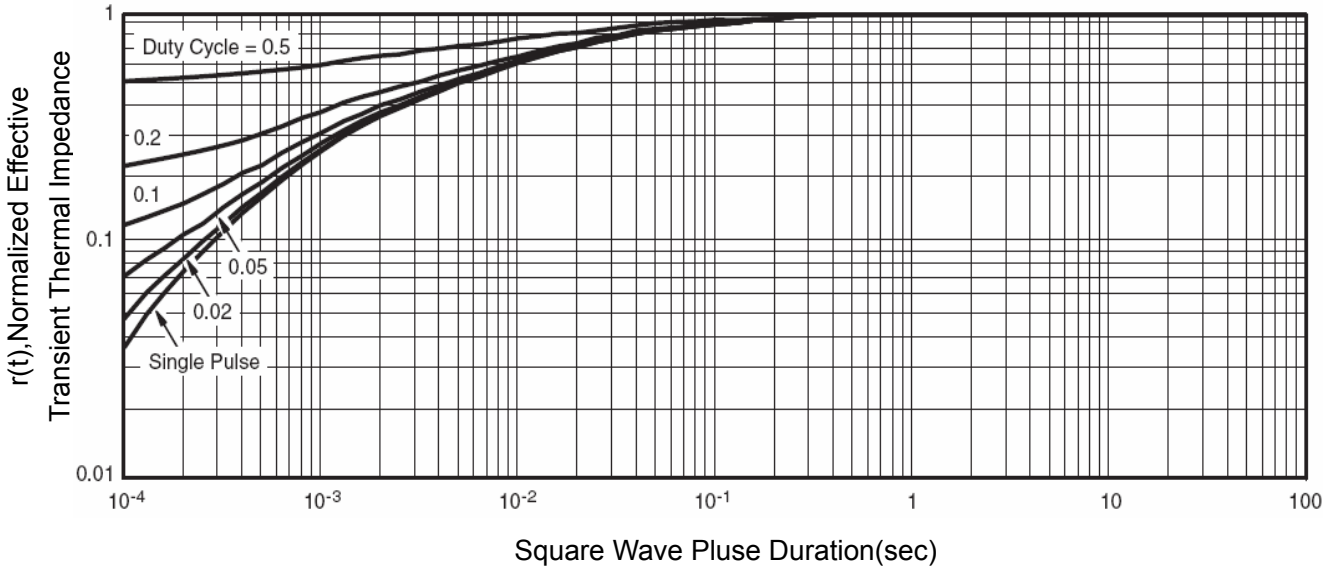
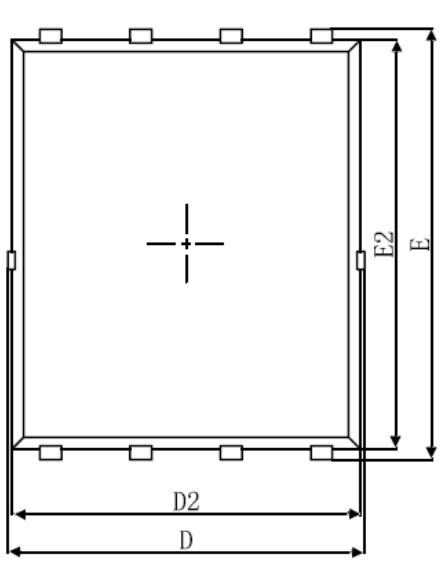
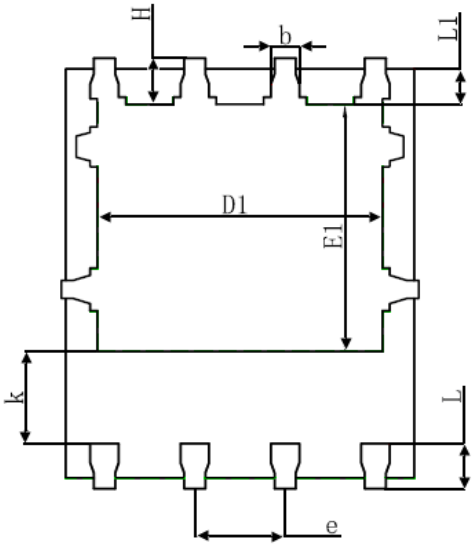


Figure 11 Normalized Maximum Transient Thermal Impedance

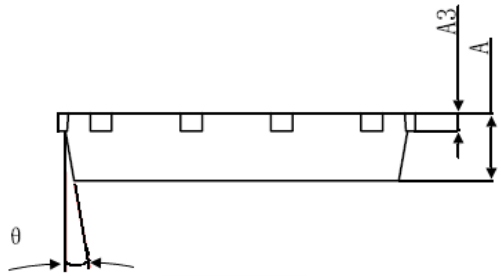
DFN5X6-8L Package Information



Top View
[顶视图]



Bottom View
[背视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	8°	12°	8°	12°

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