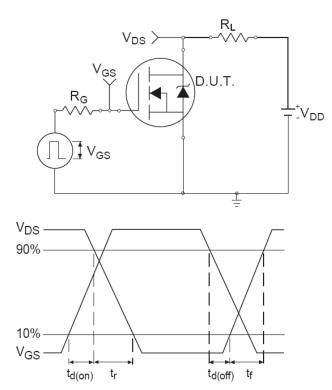
Features

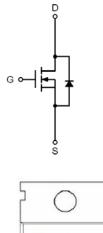
- $V_{DSS}=100V/V_{GSS}=\pm 25V/I_D=140A$ $R_{DS(ON)}=7.2m\Omega(max.)@V_{GS}=10V$
- Low Dense Cell Design
- Reliable and Rugged
- Advanced trench process technology

Applications

- Synchronous Rectification
- Power Management in Inverter System

Switching Time Test Circuit and Waveforms





Pin Description



Marking and pin Assignment



TO-220-3L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity	
PTIHF€	PTIHF€	₩₩VUËG€ËHŠ ₩₩₩				ÁÁ

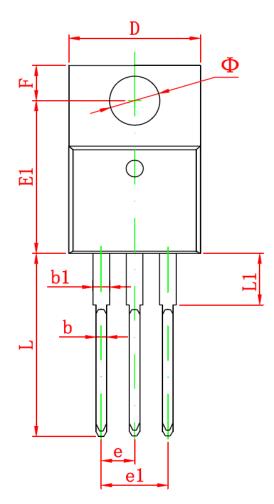
Electrical Characteristics of CP Test (TA=25°C unless otherwise noted)

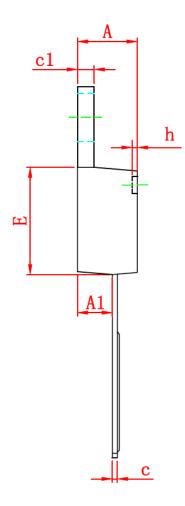
Symbol	Parameter Test Conditions		Min.	Тур	Max.	Unit
Static Chai	racteristics					
BV_{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V,I _D =250uA	100			V
I _{DSS}	Zero Gate Voltage Drain Current	V_{DS} =80V, V_{GS} =0V			1	uA
		T _J =85°C)		30	
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} ,I _D =250uA	2	2.8	4	V
I _{GSS}	Gate Leakage Current	V_{GS} =±25V, V_{DS} =0V			±100	nA
R _{DS(on)}	Drain-Source On-Resistance	V _{GS} =10V, I _D =40A		6.2	7.2	mΩ
V_{SD}	Diode Forward Voltage	I_{SD} =30A, V_{GS} =0V			1.3	V
R _G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, Frequency=1MHz		1.7		Ω

Note: 1: Pulse test ; pulse width \leq 300ns, duty cycle \leq 2%.

2: Guaranteed by design, not subject to production testing.

TO-220-3L PACKAGE OUTLINE DIMENSIONS





Symbol	Dimensions	In Millimeters	Dimensions In Inches		
Symbol	Min	Мах	Min	Мах	
A	4.470	4.670	0.176	0.184	
A1	2.520	2.820	0.099	0.111	
b	0.710	0.910	0.028	0.036	
b1	1.170	1.370	0.046	0.054	
С	0.310	0.530	0.012	0.021	
c1	1.170	1.370	0.046	0.054	
D	10.010	10.310	0.394	0.406	
E	8.500	8.900	0.335	0.350	
E1	12.060	12.460	0.475	0.491	
e	2.540) TYP	0.100 TYP		
e1	4.980	5.180	0.196	0.204	
F	2.590	2.890	0.102	0.114	
h	0.000	0.300	0.000	0.012	
L	13.400	13.800	0.528	0.543	
L1	3.560	3.960	0.140	0.156	
Φ	3.735	3.935	0.147	0.155	

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