

P-Channel Enhancement Mode Power MOSFET

Description

The HM4487 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. It is ESD protested.

General Features

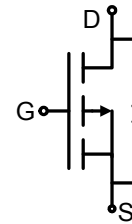
- $V_{DS} = -100V, I_D = -4.5A$
 $R_{DS(ON)} < 100m\Omega @ V_{GS} = -10V$ (Typ: 85m Ω)
- Super high dense cell design
- Advanced trench process technology
- Reliable and rugged
- High density cell design for ultra low On-Resistance

Application

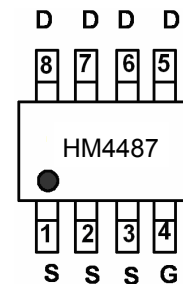
- Power management in notebook computer
- Portable equipment and battery powered systems

100% UIS TESTED!

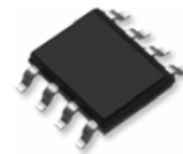
100% ΔV_{ds} TESTED!



Schematic diagram



Marking and pin Assignment



SOP-8 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM4487	HM4487	SOP8	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-4.5	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	-3.0	A
Pulsed Drain Current	I_{DM}	-18	A
Maximum Power Dissipation	P_D	3	W
Derating factor		0.56	W/ $^\circ C$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta jc}$	1.79	$^{\circ}\text{C/W}$
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

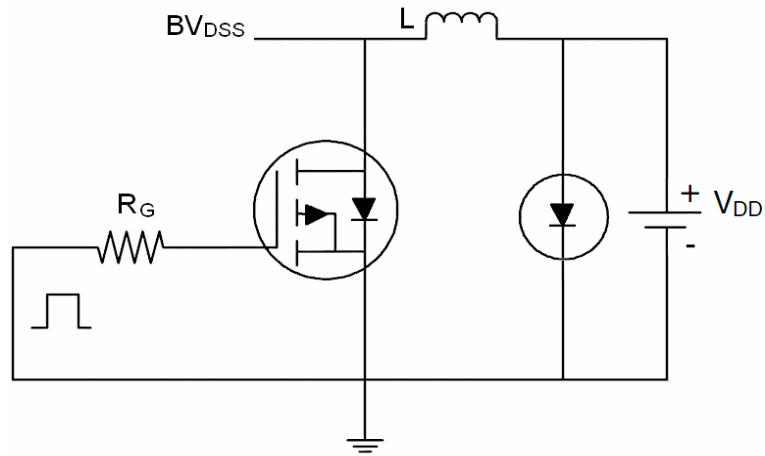
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =-250μA	-100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-100V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±20	μA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =-250μA	-1	-1.9	-3	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-4.5A	-	85	100	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-50V,I _D =-4.5A	5	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =-25V,V _{GS} =0V, F=1.0MHz	-	2100	-	PF
Output Capacitance	C _{oss}		-	590	-	PF
Reverse Transfer Capacitance	C _{rss}		-	140	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-50V,I _D =-4.5A V _{GS} =-10V,R _{GEN} =9.1Ω	-	16	-	nS
Turn-on Rise Time	t _r		-	73	-	nS
Turn-Off Delay Time	t _{d(off)}		-	34	-	nS
Turn-Off Fall Time	t _f		-	57	-	nS
Total Gate Charge	Q _g	V _{DS} =-80V,I _D =-4.5A, V _{GS} =-10V	-	61	-	nC
Gate-Source Charge	Q _{gs}		-	14	-	nC
Gate-Drain Charge	Q _{gd}		-	29	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V,I _S =-4.5A	-	-	-1.2	V
Diode Forward Current (Note 2)	I _S	-	-	-	-4.5	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F =-4.5A di/dt = 100A/μs(Note3)	-	88.3	-	nS
Reverse Recovery Charge	Q _{rr}		-	65.9	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

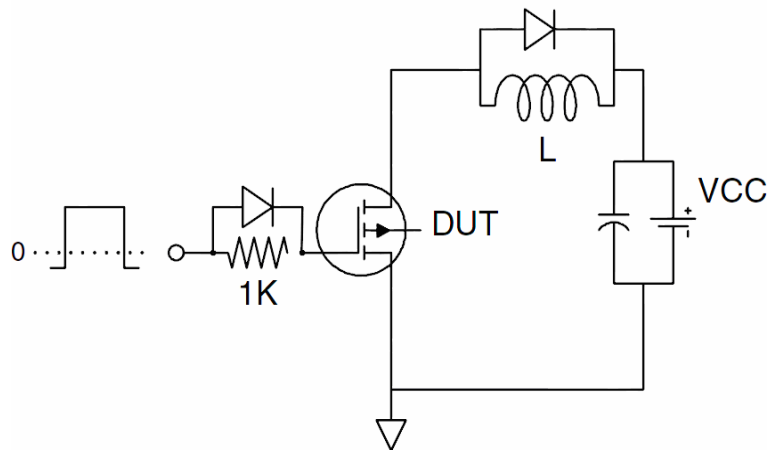
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=-50V, V_G=-10V, L=0.5mH, R_g=25\Omega$

Test Circuit

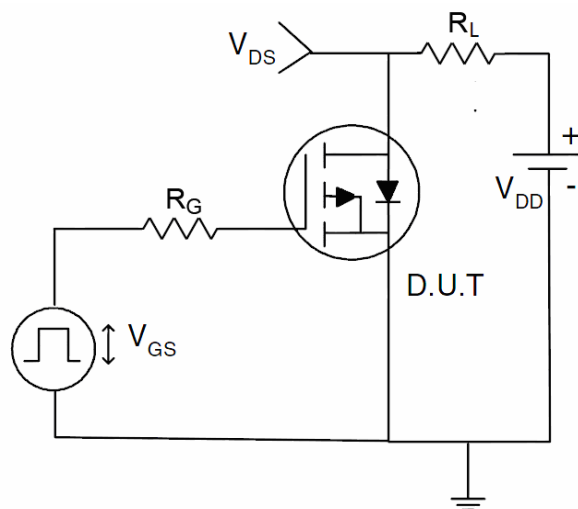
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

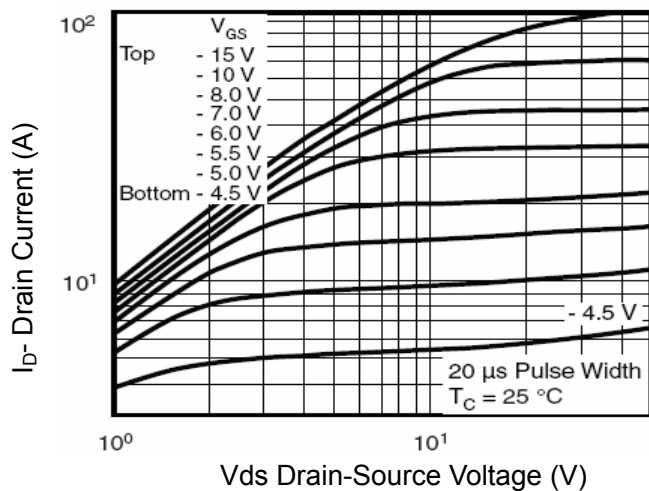


Figure 1 Output Characteristics

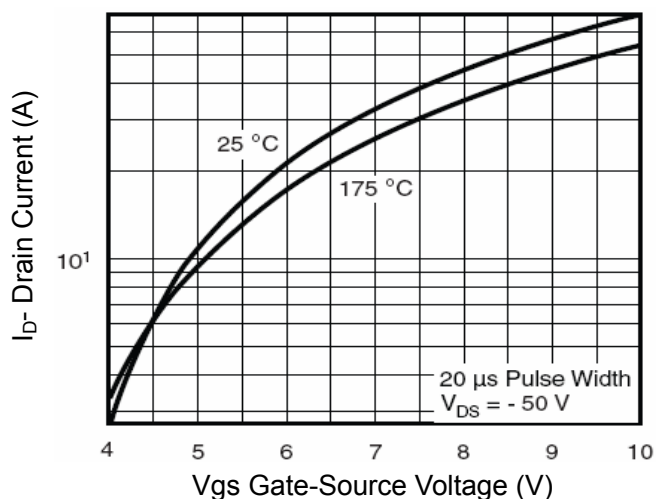


Figure 2 Transfer Characteristics

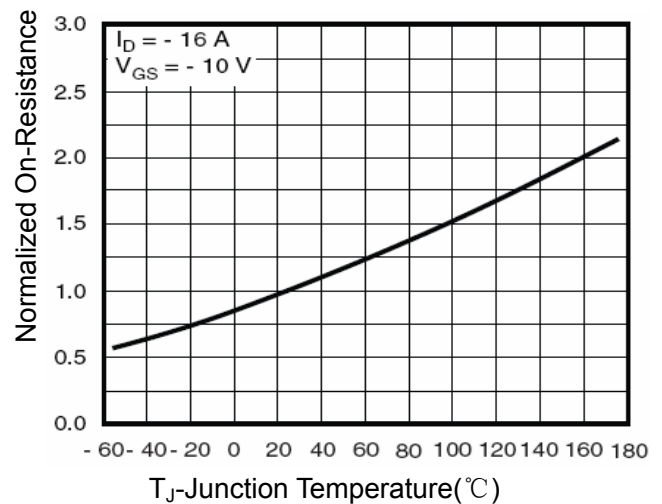


Figure 4 $R_{DS(on)}$ -Junction Temperature

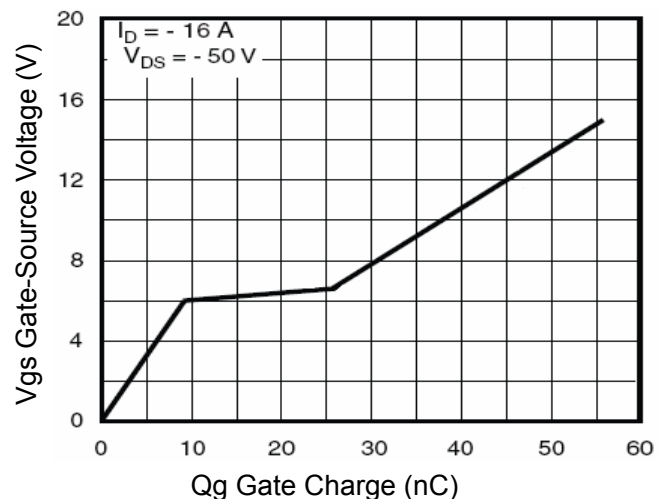


Figure 5 Gate Charge

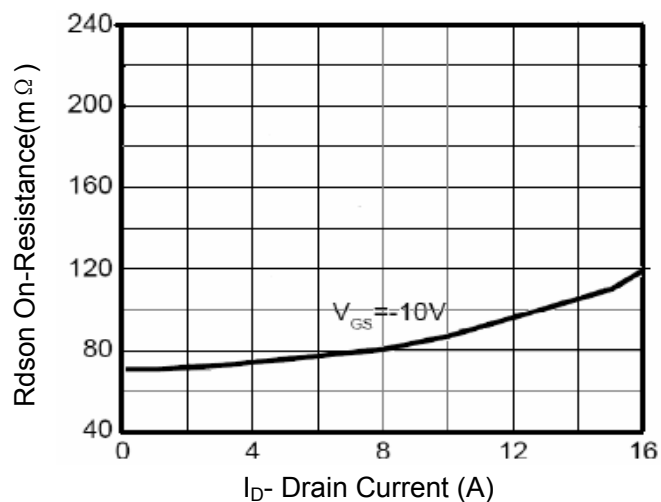


Figure 3 $R_{DS(on)}$ - Drain Current

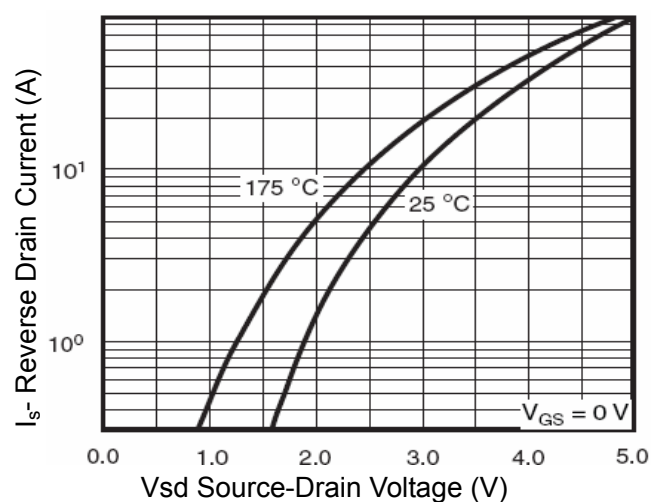


Figure 6 Source- Drain Diode Forward

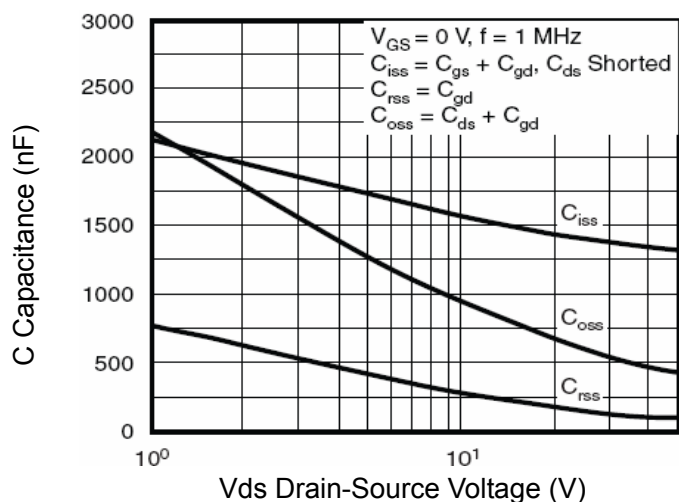


Figure 7 Capacitance vs Vds

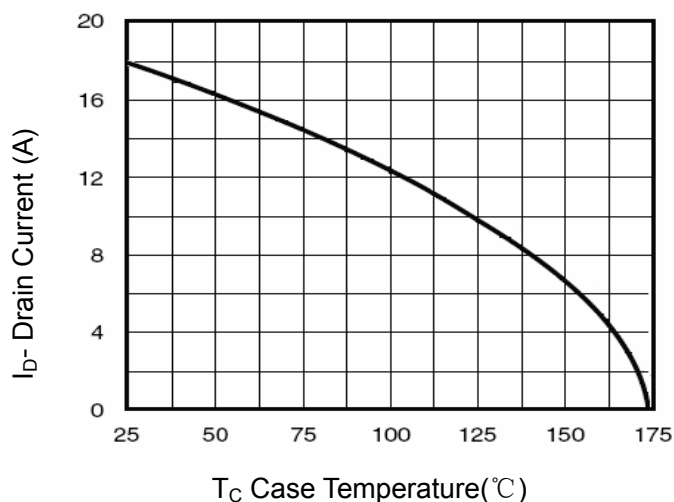


Figure 9 Drain Current vs Case Temperature

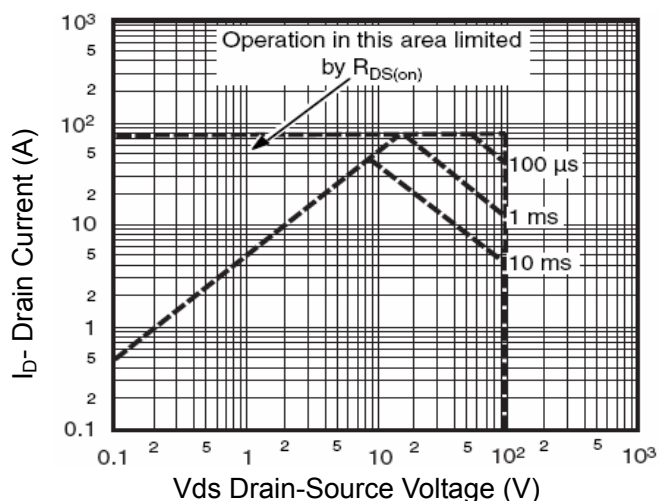


Figure 8 Safe Operation Area

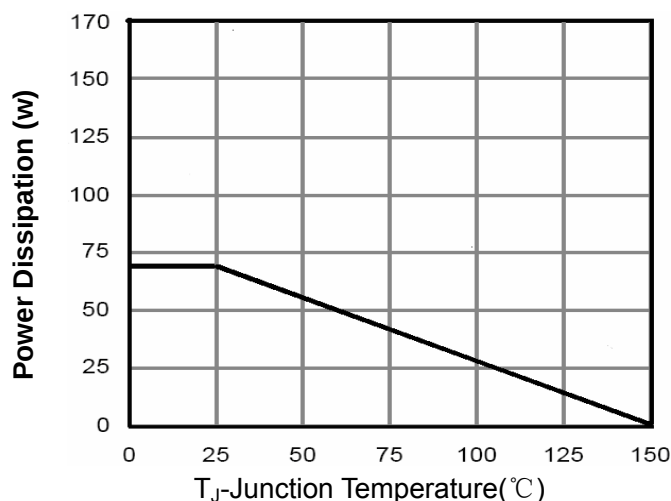


Figure 10 Power De-rating

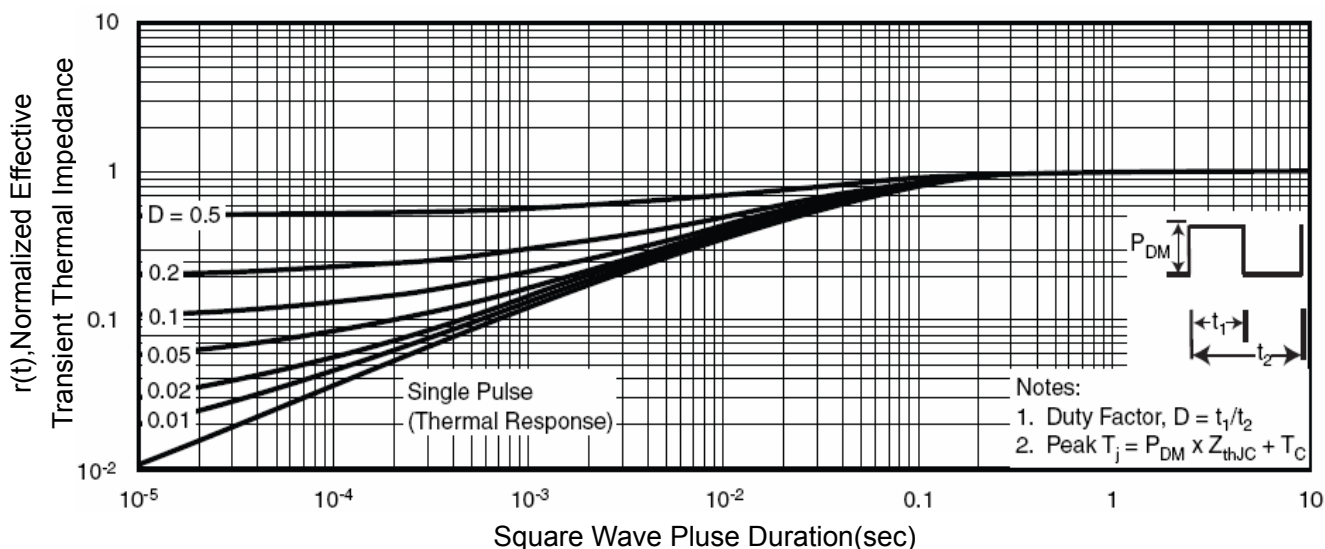
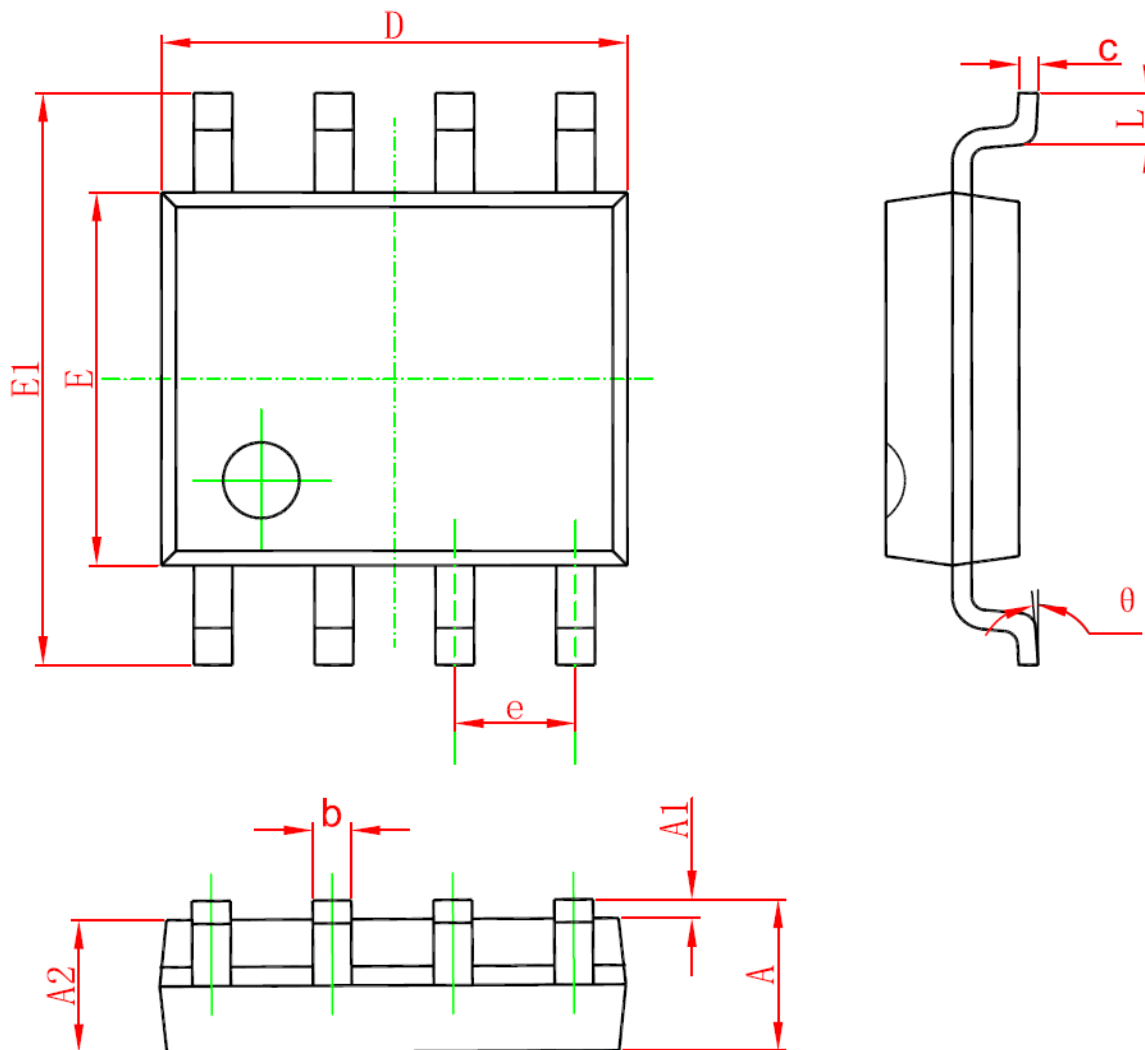


Figure 11 Normalized Maximum Transient Thermal Impedance

SOP-8 PACKAGE IN FORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°