

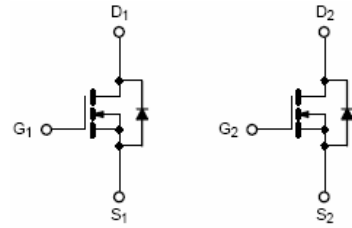
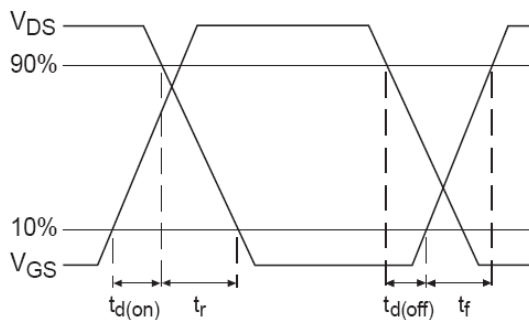
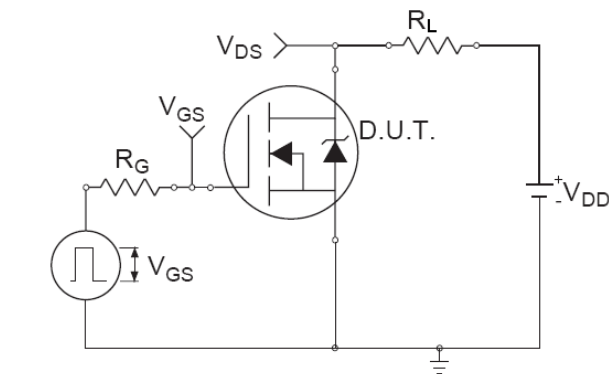
Features

- $V_{DS}=100V/V_{GS}=\pm 20V/I_D=6.5A$
 $R_{DS(ON)}=37m\Omega(max.)@V_{GS}=10V$
- Reliable and Rugged
- Advanced trench process technology
- High Density Cell Design For Low On-Resistance

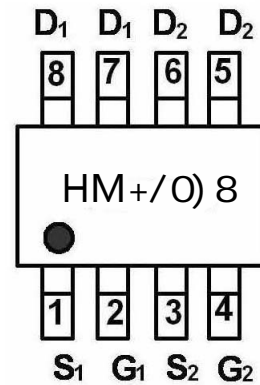
Applications

- Power Management in Inverter System
- Boost for LED Backlight

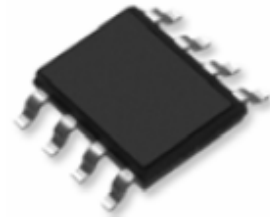
Switching Time Test Circuit and Waveforms



Schematic diagram



Marking and pin Assignment



SOP-8 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
PTI JGE	PTI JGE	UUI	-	-	

Absolute Maximum Ratings (T_A=25°C unless otherwise noted)

Symbol	Parameter	Typical	Unit
V _{DSS}	Drain-Source Voltage	100	V
V _{GSS}	Gate –Source Voltage	±20	V
I _D	Continuous Drain Current	T _C =100°C 6.5 4.5	A A
I _{DP}	300us Pulsed Drain Current Tested	T _C =25°C 20	A
I _S	Diode Continuous Forward Current	6.5	A
T _J	Operating Junction Temperature	150	°C
T _{STG}	Storage Temperature Range	-55 ~ 150	°C

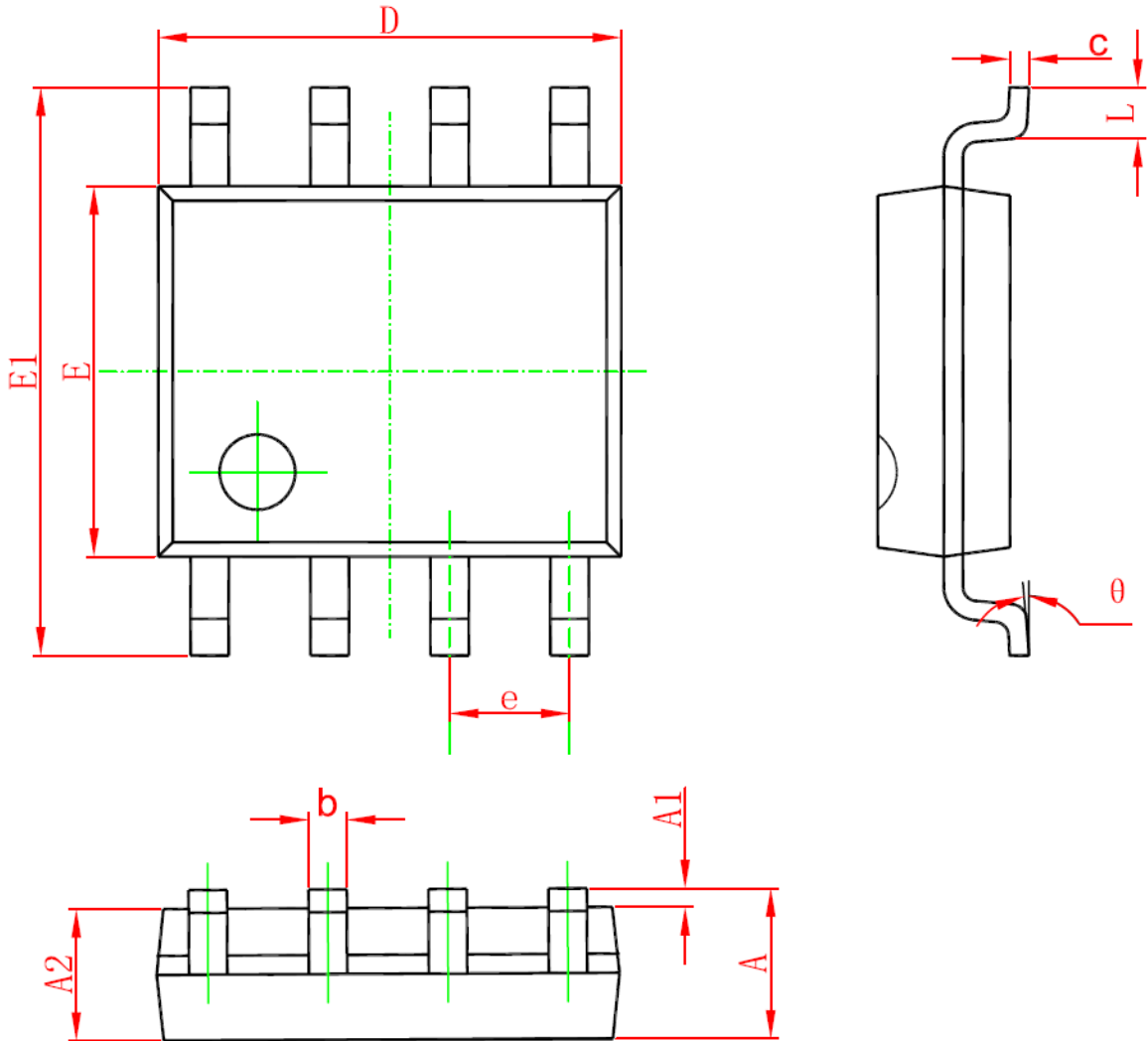
Electrical Characteristics (T_A=25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V,I _D =250uA	100			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =80V,V _{GS} =0V T _J =125°C			1 100	uA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} ,I _D =250uA	2	3.3	4	V
I _{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V			±100	nA
R _{DS(on)} ¹	Drain-Source On-Resistance	V _{GS} =10V, I _D =6.5A		33	37	mΩ
Diode Characteristics						
V _{SD} ¹	Diode Forward Voltage	I _{SD} =6.5A,V _{GS} =0V			1.1	V
t _{rr}	Reverse Recovery Time	I _{SD} =6.5A,		60		ns
Q _{rr}	Reverse Recovery Charge	dif/dt=100A/us		90		nC
Dynamic Characteristics ²						
R _G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, Frequency=1MHz		1.4		Ω
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =30V Frequency=1MHz		2000		pF
C _{oss}	Output Capacitance			450		
C _{rss}	Reverse Transfer Capacitance			260		
t _{d(on)}	Turn-On Delay Time	V _{DD} =50V, R _L =30Ω I _D =1.0A, V _{GEN} =10V R _G =6Ω		25		ns
t _r	Turn-On Rise Time			18		
t _{d(off)}	Turn-Off Delay Time			60		
t _f	Turn-Off Fall Time			78		
Gate Charge Characteristics ²						
Q _g	Total Gate Charge	V _{DS} =50V, V _{GS} =10V I _D =6.5A		50		nC
Q _{gs}	Gate-Source Charge			13.5		
Q _{gd}	Gate-Drain Charge			11		

Note:

- 1: Pulse test ; pulse width ≤ 300ns, duty cycle ≤ 2%.
 2: Guaranteed by design, not subject to production testing.

SOP-8 PACKAGE IN FORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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