

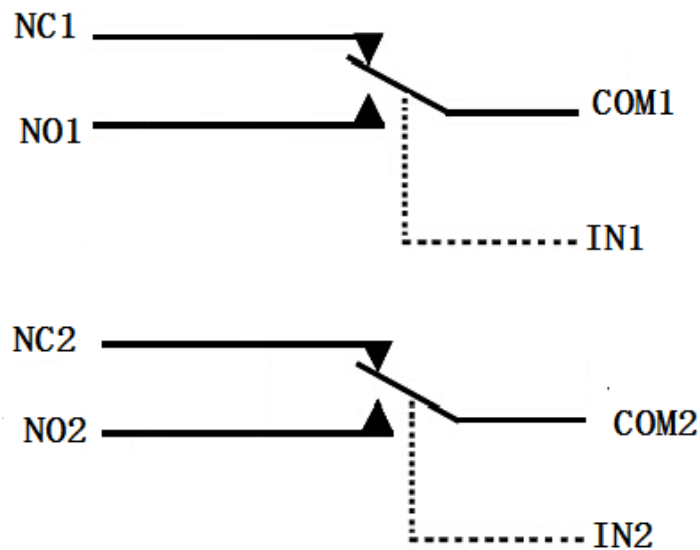
## 0.5 $\Omega$ Dual SPDT Negative Signal Handling Analog Switch

### General Description

The HM5228 is an advanced CMOS analog switch fabricated in Sub-micron silicon gate CMOS technology. The part also features guaranteed Break Before Make (BBM) switching, assuring the switches never short the driver. The switches can handle negative signal down to -2V.

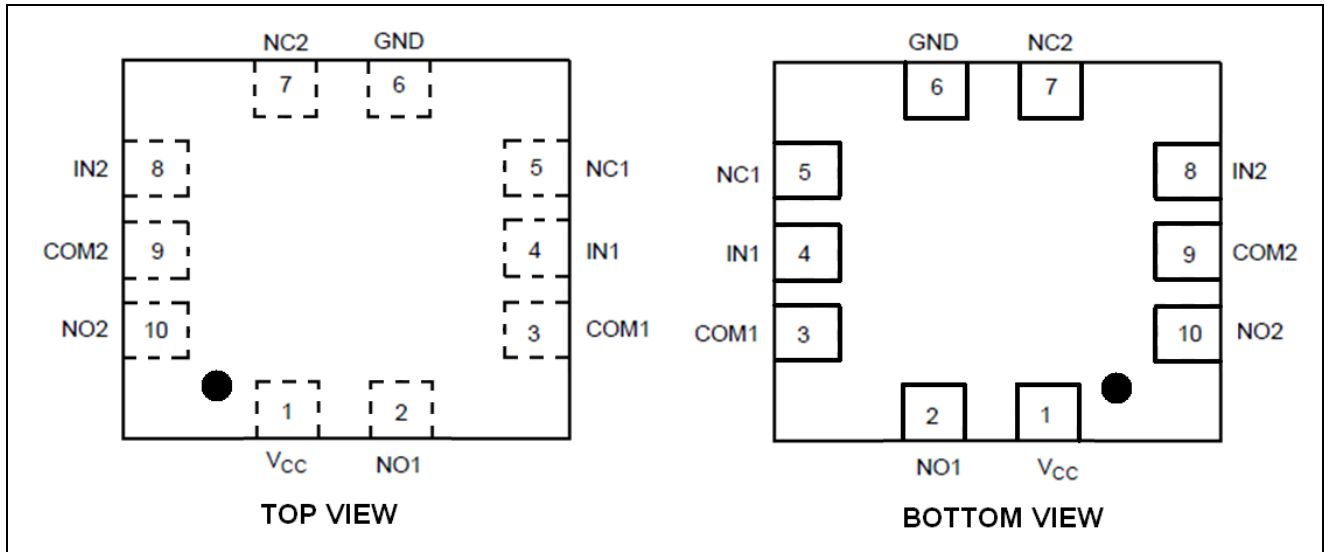
### Features

- Low RON: typical 0.5 $\Omega$  @  $V_{CC}=5V$
- Single Supply Operation from 2.5V-5V
- Full -2V- $V_{CC}$  Signal Handling Capability
- High Off-Channel Isolation
- Low Standby Current
- Low Distortion
- Break-Before-Make(BBM) switching
- High Continuous Current Capability:  $\pm 300$  mA Through Each Switch
- Applications in Cell Phone Audio Block/ Speaker and Earphone Switching Ring-Tone Chip / Amplifier Switching/Modems
- Package :QFN10L(1.8\*1.4)



Analog Symbol

### Pin Configuration



### Pin Function

QFN PIN #	Symbol	FUNCTION
1	VCC	Power supply
2	NO1	Independent Channels
3	COM1	Common Channels
4	IN1	Controls
5	NC1	Independent Channels
6	GND	Ground (V)
7	NC2	Independent Channels
8	IN2	Controls
9	COM2	Common Channels
10	NO2	Independent Channels

### Truth Table

IN1, 2	NO1, 2	NC1, 2
0	OFF	ON
1	ON	OFF

### Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit
Supply Voltage	V <sub>CC</sub>	-0.5~+6.0	V
Analog Input Voltage	V <sub>IS</sub>	-2.5~V <sub>CC</sub> +0.3  V <sub>CC</sub> -V <sub>IS</sub>   <6.5V	V
Digital Select Input Voltage	V <sub>IN</sub>	-0.5~+6.0	V
Output Voltage	V <sub>O</sub>	-2.5~V <sub>CC</sub> +0.3  V <sub>CC</sub> -V <sub>O</sub>   <6.5V	V
Continuous DC Current from COM to NC/NO	I <sub>an1</sub>	±300	mA
Peak Current from COM to NC/NO, 10 duty cycle (Note 1)	I <sub>an1-pk1</sub>	±500	mA
Continuous DC Current into COM/NO/NC with respect to V <sub>CC</sub> or GND	I <sub>clmp</sub>	±100	mA

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

Note1. Defined as 10% ON, 90% off duty cycle.

Characteristic	Symbol	Min	Max	Unit
DC Supply Voltage	V <sub>CC</sub>	2.5	5	V
Digital Select Input Voltage	V <sub>IN</sub>	GND	5	V
Analog Input Voltage	V <sub>IS</sub>	-2	V <sub>CC</sub>	V
Operating Temperature Range	T <sub>A</sub>	-45	+85	°C
Input Rise or Fall Time, SELECT	t <sub>r</sub> ,t <sub>f</sub>	0	20	ns/V

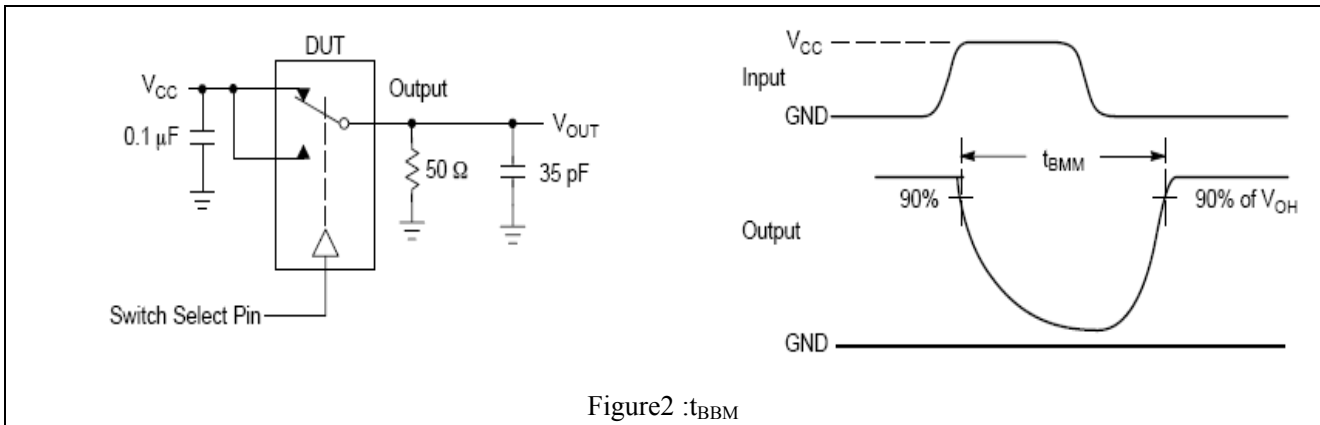
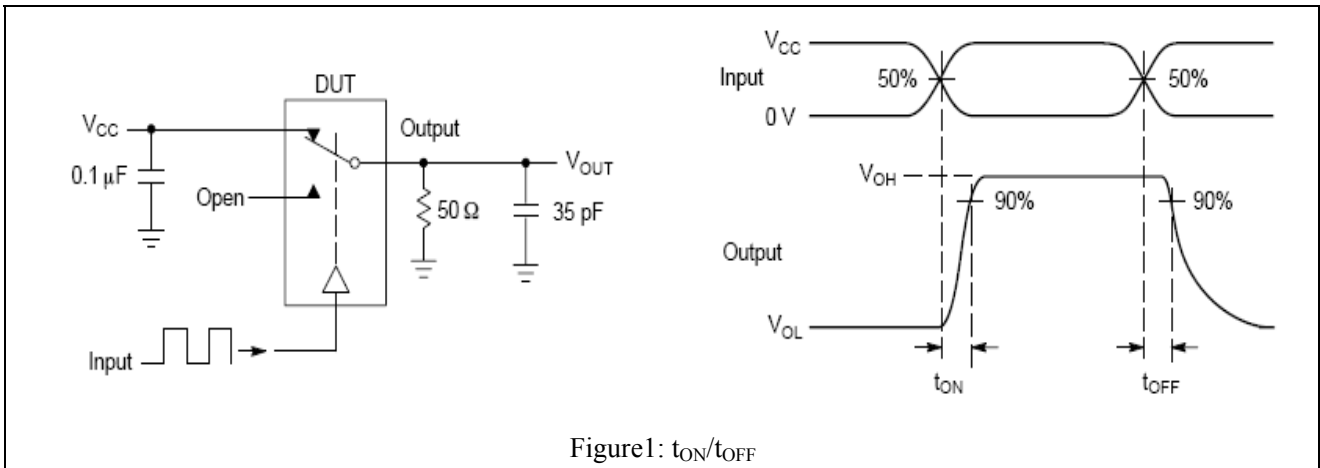
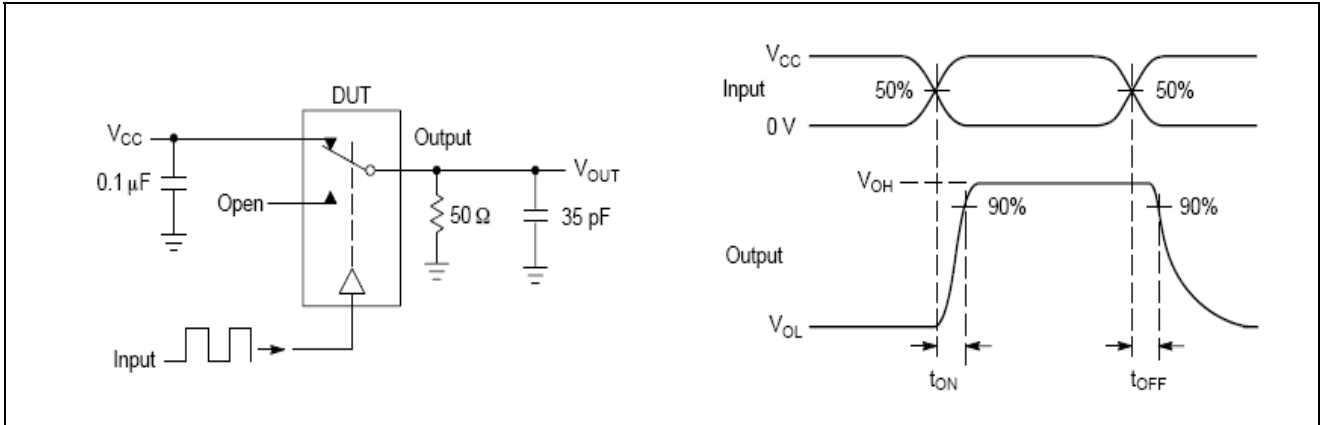
### Electrical Characteristics

Symbol	Parameter	Test Conditions	V <sub>CC</sub> ±10%	T <sub>A</sub> =25°C			Unit
				Min	Typ	Max	
V <sub>IH</sub>	High-Level Input Voltage, Select Inputs		2.5~5	1.3			V
V <sub>IL</sub>	Low-Level Input Voltage, Select Inputs		2.5~5			0.5	V
I <sub>IN</sub>	Maximum Input Leakage Current, Select Inputs	V <sub>IN</sub> =V <sub>CC</sub> or GND	5			±0.3	uA
I <sub>OFF</sub>	Power Off Leakage Current	V <sub>IN</sub> =V <sub>CC</sub> or GND	0			±0.5	uA
I <sub>CC</sub>	Maximum Quiescent Supply Current (Note 2)	SELECT, V <sub>IS</sub> =V <sub>CC</sub> or GND	3.6			1	uA
I <sub>COM(ON)</sub>	COM ON leakage Current	V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub> ,	5	-20		20	nA

	(Note 3)	$V_{NO}=0.3V$ or $4.7V$ $V_{NC}$ floating $V_{NC}=0.3V$ or $4.7V$ $V_{No}$ floating $V_{COM}=0.3V$ or $4.7V$					
$R_{ON}$	On-Resistance (Note 2, Note 3)	$V_{IS}=GND$ to $V_{CC}$ $I_{IN}=100mA$	5		0.4	0.5	$\Omega$
			3.3		0.6	0.7	
			2.0		1.5	1.7	
$R_{FLAT}$	On-Resistance Flatness (Note 2, Note 3, Note 5)	$I_{COM}=100mA$ $V_{IS}=GND$ to $V_{CC}$	5			0.3	$\Omega$
$\Delta R_{ON}$	On-Resistance Match Between Channels (Note 2, Note 3, Note 4)	$I_{COM}=100mA$ $V_{IS}=1.5V$	5		0.25		$\Omega$
$t_{ON}$	Turn-On Time (Figure 1)	$V_{IS}=1.5V$	2.5~3.3		35	45	ns
			2.5~5.0		25	30	
$t_{OFF}$	Turn-Off Time (Figure 1)	$V_{IS}=1.5V$	2.5~3.3		17	20	ns
			3.6~5.0		15	20	
$t_{BBM}$	Break-Before-Make Time (Note 6) (Figure 2)	$C_L=35pF, R_{IS}=50\Omega$ $V_{IS}=1.5V$	2.5~3.3	7	9		ns
			3.6~5.0	4	6		
BW	On-Channel -3dB Bandwidth or Frequency Response (Figure 4)	$R_{IS}=50\Omega$	2.5~5.0		50		MHz
$V_{ISO}$	Off-Channel Isolation (Figure 4)	$F_{IS}=100kHz,$ $V_{IN}=GND$ to $V_{CC}$ $C_L=5pF, R_L=50\Omega$ $V_{IS}=1V$ RMS	2.5~5.0		-66		dB
Q	Charge Injection Select Input to Common I/O (Figure 3)	$V_{IN}=0$ or $V_{CC}$ $R_{IS}=0\Omega, C_L=100pF$ $R_L=1M\Omega$ $Q=C_L \times \Delta V_{Out}$	2.5~3.3		51		pC
			3.6~5.0		49		
THD	Total Harmonic Distortion THD + Noise	$F_{IS}=20Hz$ to $20KHz$ $R_L=600\Omega, C_L=50pF$ $V_{IS}=2V$ RMS	3.6		0.08		%
$V_{CT}$	Channel-to-Channel Crosstalk (Figure 4)	$F_{IS}=100KHz,$ $V_{IN}=GND$ to $V_{CC}$ $R_L=50\Omega, C_L=5pF$ $V_{IS}=1V$ RMS	3.6~5.0		-72		dB
$C_{IN}$	Control Pin Input Capacitance		3.6		3.5		pF
$C_{NC}/C_{NO}$	NC/NO Port Capacitance		3.6		50		pF
$C_{COM}$	COM Port Capacitance When Switch is Enabled		3.6		120		pF

Note 2. Guaranteed by design

3. Guaranteed by design. Resistance measurements do not include test circuit or package resistance
4.  $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$  between NC1 and NC2 or between NO1 and NO2.
5. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.
6. Guaranteed by design in  $-40^{\circ}\text{C}$ .



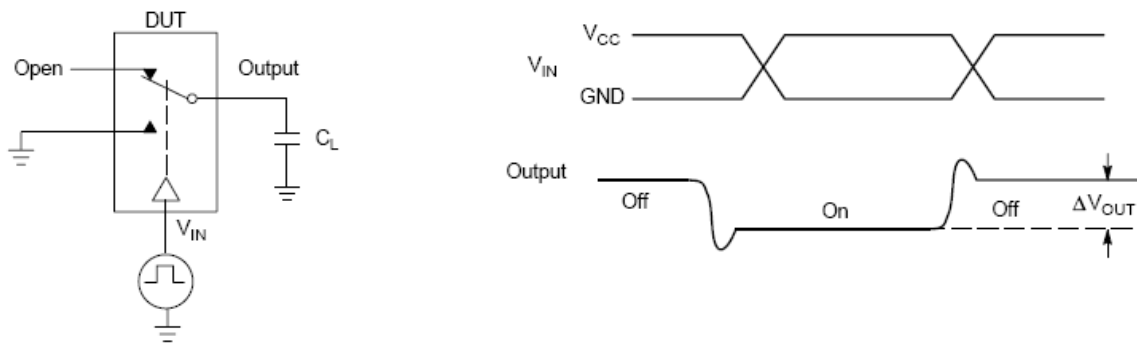
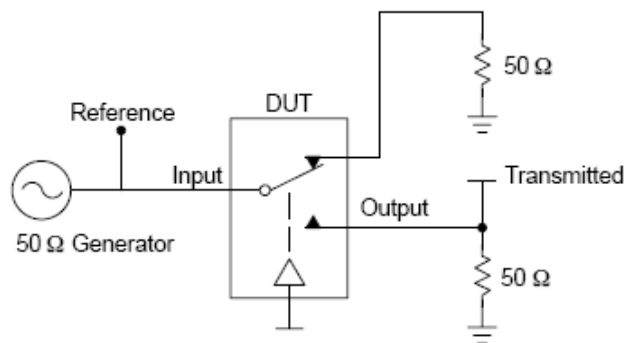


Figure3: Charge Injection



$$V_{ISO}=20\log (V_{OUT}/V_{IN})$$

$$V_{ONL}=20\log (V_{OUT}/V_{IN})$$

$$V_{CT}=20\log (V_{OUT}/V_{IN})$$

BW=the frequency 3dB below  $V_{ONL}$

Figure 4. -3dB Bandwidth/Off Channel Isolation/On Channel Loss(BW)/Crosstalk  
 (On Channel to Off Channel)/ $V_{ONL}$

Package Dimension

QFN10L

