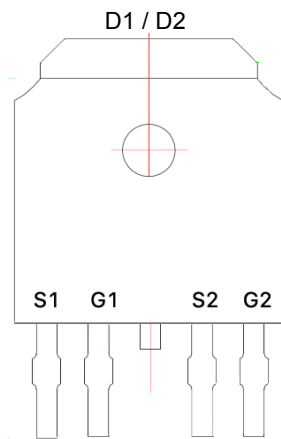


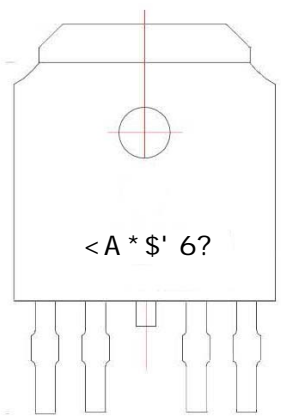
DESCRIPTION

The HM603BK is the N & P-Channel enhancement mode power field effect transistor using high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance and provide superior switching performance. This device is particularly suited for low voltage application such as power management, where high-side switching, low in-line power loss and resistance to transient are needed.

PIN CONFIGURATION TO252-4L



PART MARKING



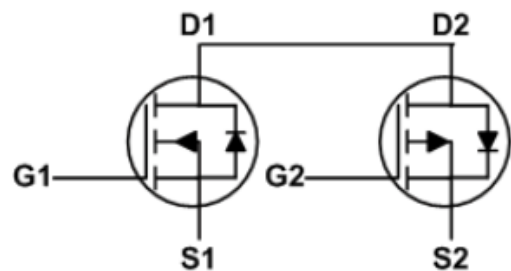
FEATURE

N-Channel

- 60V/8.0A, $R_{DS(ON)} = 37m\Omega$
@ $V_{GS} = 10V$
- 60V/5.0A, $R_{DS(ON)} = 28m\Omega$
@ $V_{GS} = 4.5V$

P-Channel

- -60V/-5.0A, $R_{DS(ON)} = 46m\Omega$
@ $V_{GS} = -10V$
- -60V/-3.0A, $R_{DS(ON)} = 65m\Omega$
@ $V_{GS} = -4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO252-4L package



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter		Symbol	Typical		Unit
			N	P	
Drain-Source Voltage		V _{DSS}	60	-60	V
Gate-Source Voltage		V _{GSS}	±20	±20	V
Continuous Drain Current	T _A =25°C	I _D	23.0	-18.0	A
	T _A =70°C		15.0	-11.0	
Pulsed Drain Current		I _{DM}	46	-36	A
Continuous Source Current (Diode Conduction)		I _S	59	-50	A
Power Dissipation	T _A =25°C	P _D	34.7	34.7	W
Operation Junction Temperature		T _J	150		°C
Storage Temperature Range		T _{STG}	-55/150		°C
Thermal Resistance-Junction to Ambient		R _{θJA}	85	85	°C/W

ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=10mA$ $V_{GS}=0V, I_D=-10mA$	N P	60 -60		V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250 \mu A$ $V_{DS}=V_{GS}, I_D=-250\mu A$	N P	1.0 -1.0	2.5 -2.5	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$ $V_{DS}=0V, V_{GS}=\pm 20V$	N P		± 100 ± 100	nA
Zero Gate Voltage Drain Current	I_{DSS} $T_J=25^\circ C$ $T_J=55^\circ C$	$V_{DS}=48V, V_{GS}=0V$	N		1	uA
		$V_{DS}=-48V, V_{GS}=0V$	P		-1	
		$V_{DS}=32V, V_{GS}=0V$	N		5	
		$V_{DS}=-32V, V_{GS}=0V$	P		-5	
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=8.0A$	N		0.037	Ω
		$V_{GS}=-10V, I_D=-5.0A$	P		0.046	
		$V_{GS}=4.5V, I_D=5.0A$	N		0.028	
		$V_{GS}=-4.5V, I_D=-3.0 A$	P		0.065	
Forward Tran Conductance	g_{fs}	$V_{DS}=5V, I_D=8.0A$	N		21	S
		$V_{DS}=-5V, I_D=-5.0A$	P		15	
Diode Forward Voltage	V_{SD}	$I_S=1.0A, V_{GS}=0V$	N		1.2	V
		$I_S=-1.0A, V_{GS}=0V$	P		-1.2	
Dynamic						
Total Gate Charge	Q_g	N-Channel $V_{DS}=48V, V_{GS}=4.5V$ $I_D \equiv 8.0A$	N		12.6	nC
Gate-Source Charge	Q_{gs}		P		9.9	
Gate-Drain Charge	Q_{gd}	P-Channel $V_{DS}=-48V, V_{GS}=-4.5V$ $I_D \equiv -5.0A$	N		3.5	nC
			P		3.1	
Turn-On Time	$t_{d(on)}$ t_r	N-Channel $V_{DS}=30V, R_G=3.3 \Omega$ $I_D=8A, V_{GS}=10V$	N		8	nS
			P		9.7	
			N		14.2	
			P		18	
Turn-Off Time	$t_{d(off)}$ t_f	P-Channel $V_{DS}=-20V, R_G=3.3 \Omega$ $I_D=-1A, R_{GS}=-10V$	N		24.6	nS
			P		45.8	
			N		4.6	
			P		45.8	

TYPICAL CHARACTERISTICS (N MOS)

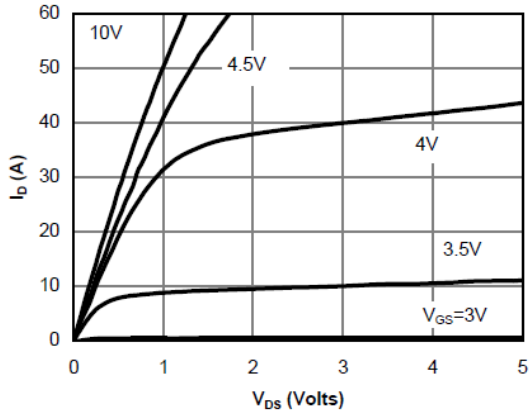


Figure 1: On-Region Characteristics (Note E)

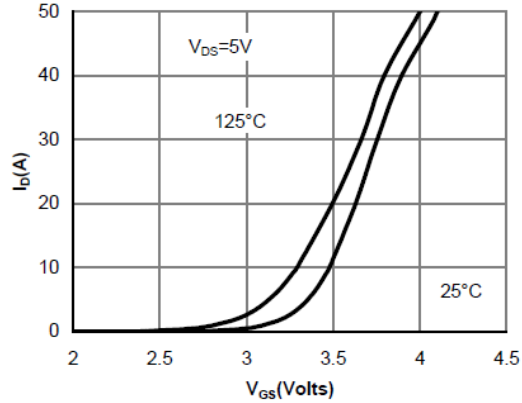


Figure 2: Transfer Characteristics (Note E)

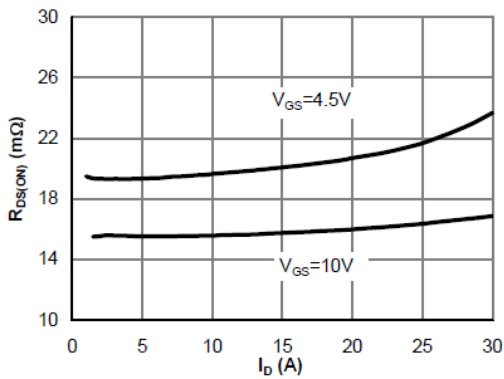


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

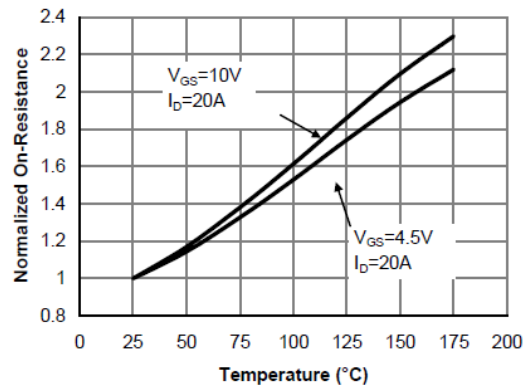


Figure 4: On-Resistance vs. Junction Temperature (Note E)

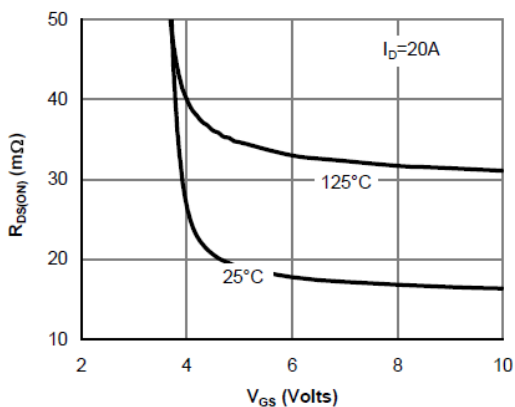


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

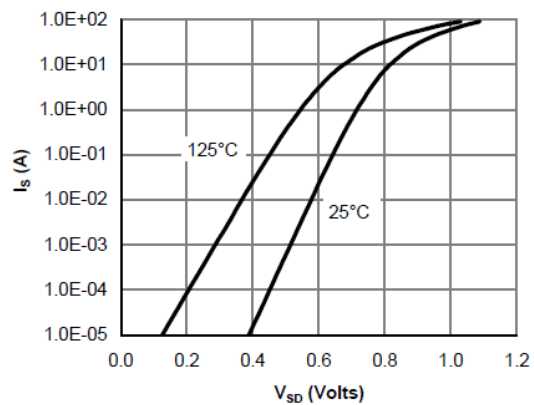


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL CHARACTERISTICS (N MOS)

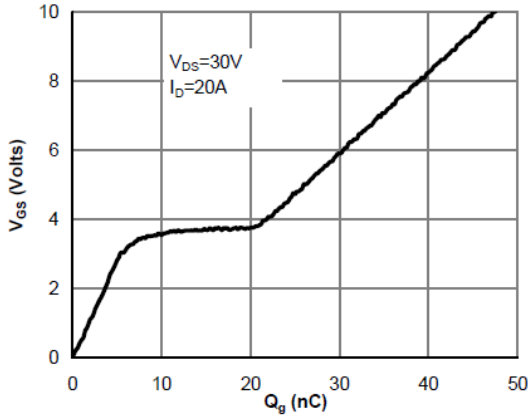


Figure 7: Gate-Charge Characteristics

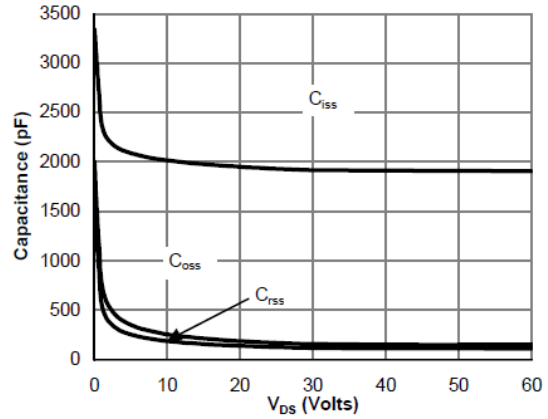


Figure 8: Capacitance Characteristics

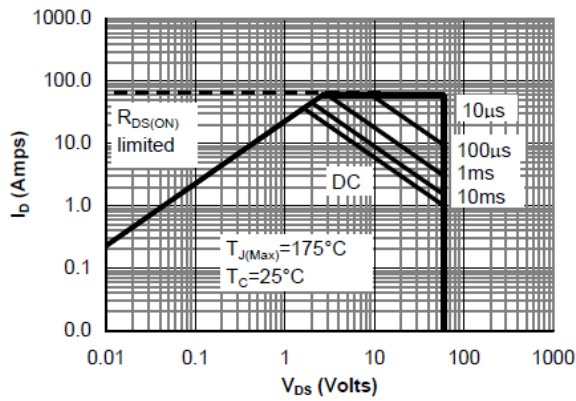


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

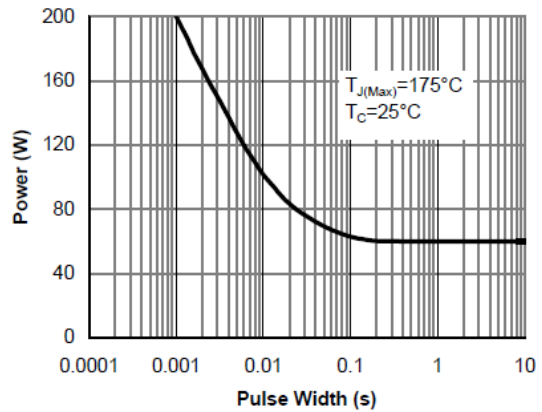


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

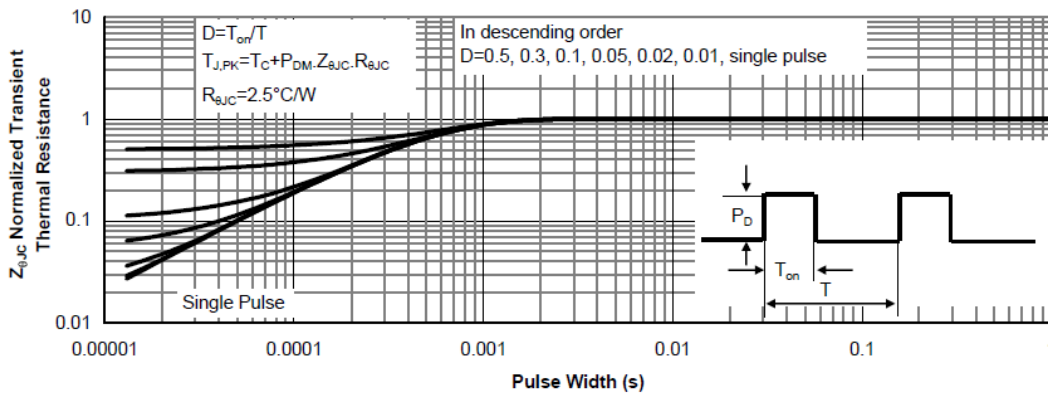


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

YPICAL CHARACTERISTICS (P MOS)

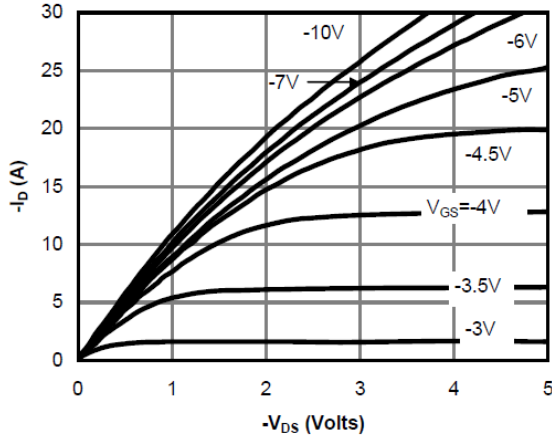


Fig 1: On-Region Characteristics

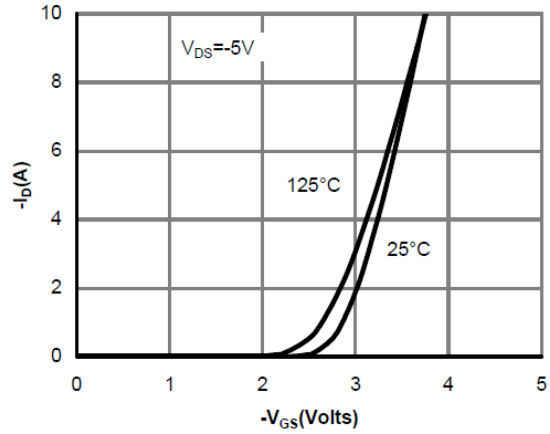


Figure 2: Transfer Characteristics

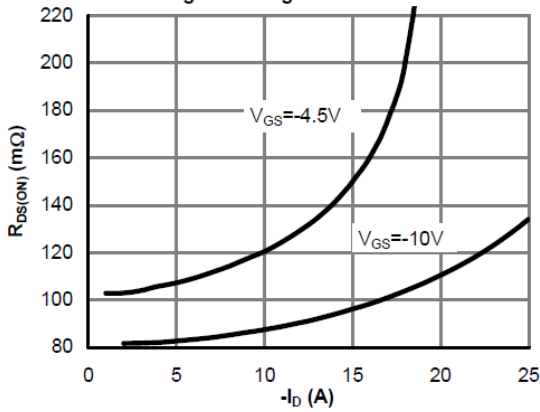


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

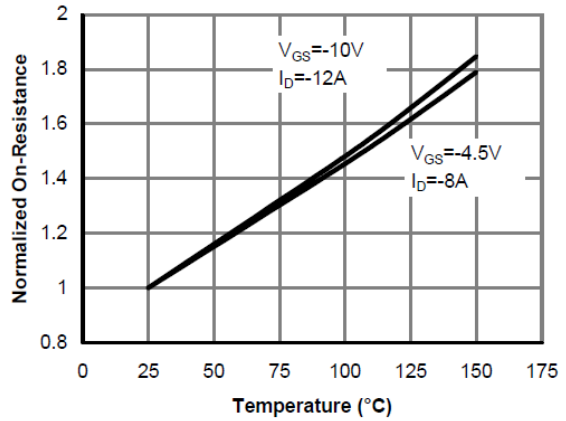


Figure 4: On-Resistance vs. Junction Temperature

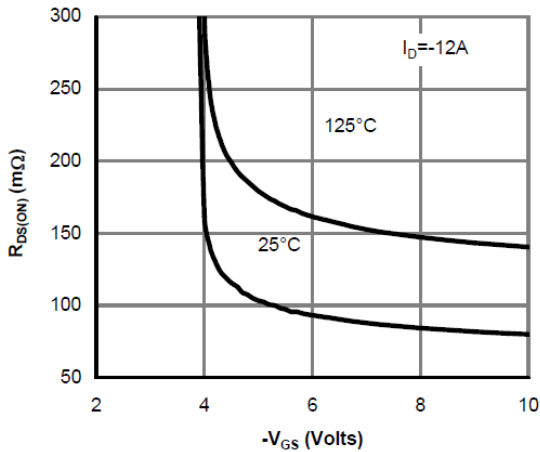


Figure 5: On-Resistance vs. Gate-Source Voltage

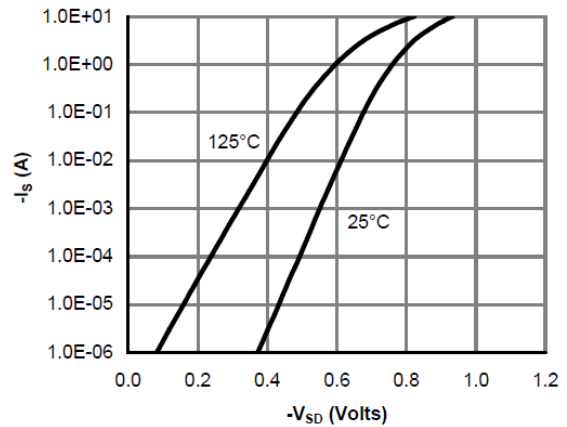


Figure 6: Body-Diode Characteristics

TYPICAL CHARACTERISTICS (P MOS)

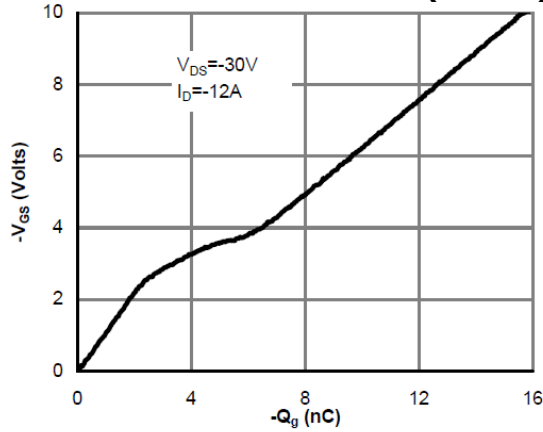


Figure 7: Gate-Charge Characteristics

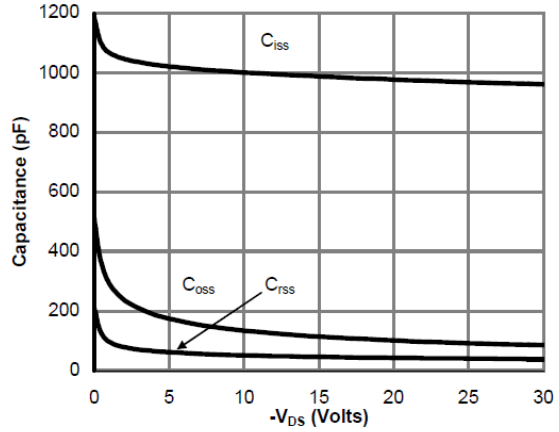


Figure 8: Capacitance Characteristics

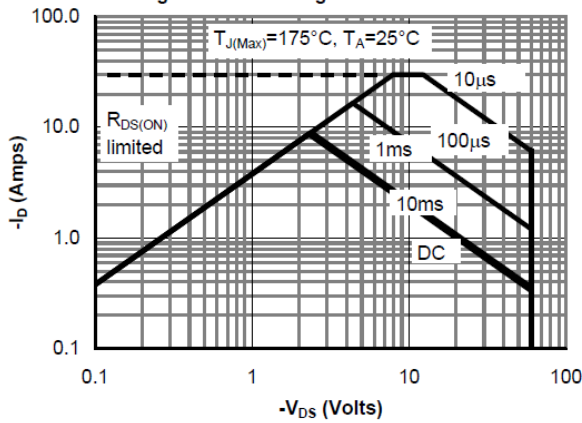


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

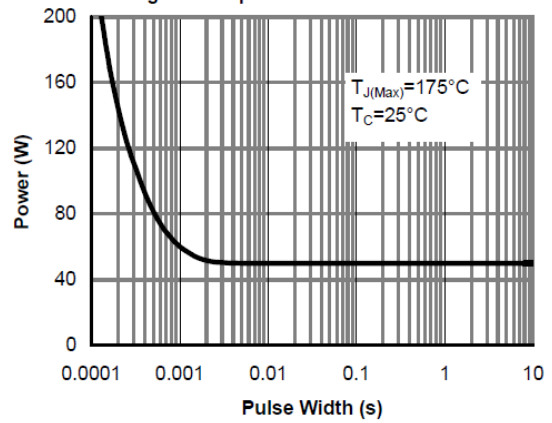


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

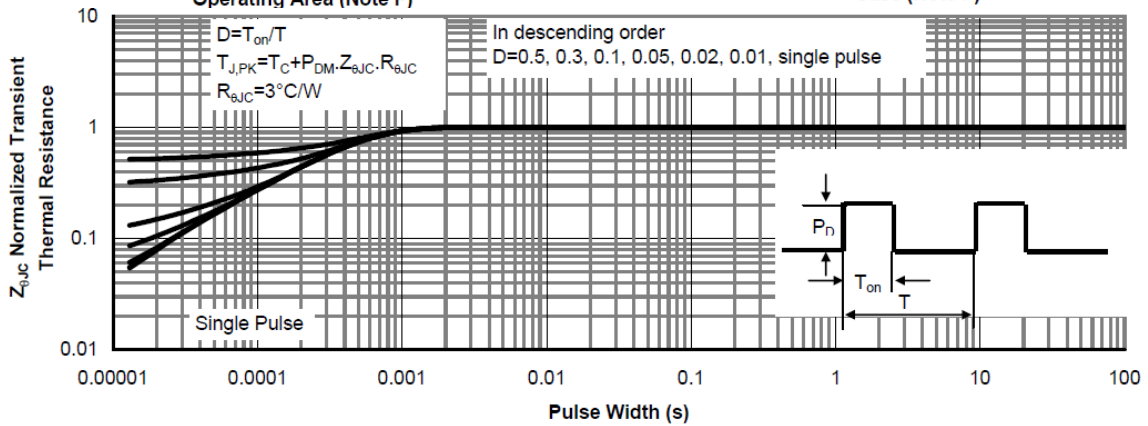


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TO252-4L PACKAGE OUTLINE

