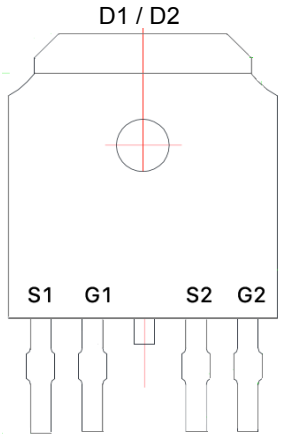
HM609BK

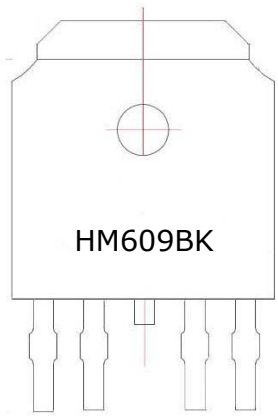
DESCRIPTION

The HM609BK is the N & P-Channel enhancement mode power field effect transistor using high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance and provide superior switching performance. This device is particularly suited for low voltage application such as power management, where high-side switching, low in-line power loss and resistance to transient are needed.

PIN CONFIGURATION
TO252-4L



PART MARKING



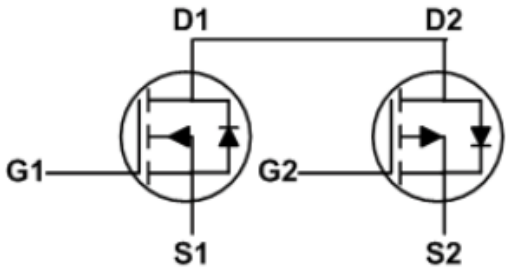
FEATURE

N-Channel

- 40V/12.0A, $R_{DS(ON)}$ = 25mR
  @V_{GS} = 10V
- 40V/10.0A, $R_{DS(ON)}$ = 32mΩ
  @V_{GS} = 4.5V

P-Channel

- -40V/-8.0A, $R_{DS(ON)}$ = 40mΩ
  @V_{GS} = -10V
- -40V/-4.0A, $R_{DS(ON)}$= 65mΩ
  @V_{GS} = - 4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO252-4L package



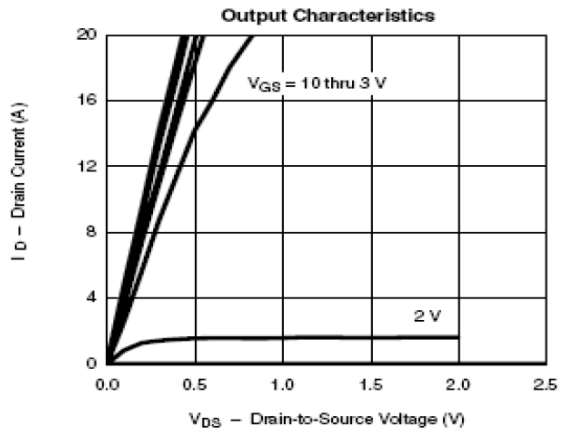
ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

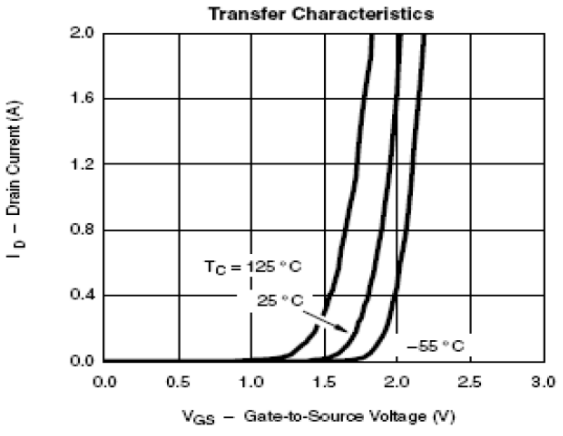
Parameter		Symbol	Typical N	Typical P	Unit
Drain-Source Voltage		V_{DSS}	40	-40	V
Gate-Source Voltage		V_{GSS}	±20	±20	V
Continuous Drain Current	T_A=25℃ T_A=70℃	I_D	23.0 18.0	-20.0 -16.0	A
Pulsed Drain Current		I_{DM}	40	-46	A
Continuous Source Current (Diode Conduction)		I_S	18	-27.5	A
Power Dissipation	T_A=25℃	P_D	25	31.5	W
Operation Junction Temperature		T_J	150		℃
Storgae Temperature Range		T_{STG}	-55/150		℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	62.5	62.5	℃/W

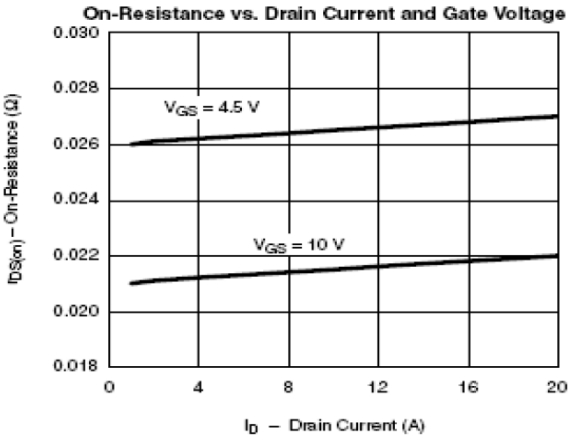
ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

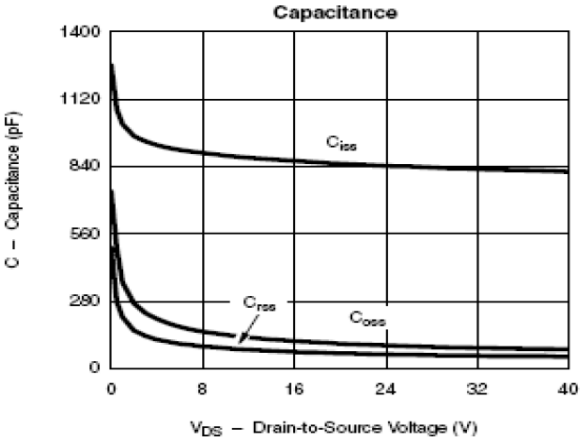
Parameter	Symbol	Condition		Min	Typ	Max	Unit
Static							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=10mA V_{GS}=0V,I_D=-10mA	N P	40 -40			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=VGS,I_D=250 uA V_{DS}=VGS,I_D=-250uA	N P	1.0 -1.0		2.5 -2.5	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V V_{DS}=0V,V_{GS}=±20V	N P			±100 ±100	nA
Zero Gate Voltage Drain Current	I_{DSS} T_J=25℃	V_{DS}=32V,V_{GS}=0V V_{DS}=-32V,V_{GS}=0V	N P			1 -1	uA
	T_J=55℃	V_{DS}=32V,V_{GS}=0V V_{DS}=-32V,V_{GS}=0V	N P			5 -5	
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=10.0A V_{GS}=-10V,I_D=-10.0A	N P		0.025 0.035	0.032 0.043	Ω
		V_{GS}=4.5V, I_D=6.0A V_{GS}=-4.5V,I_D=-5.0 A	N P		0.030 0.040	0.037 0.065	
Forward Tran Conductance	gfs	V_{DS}=5V,I_D=12.0A V_{DS}=-5V,I_D=-8.0A	N P		8 12.6		S
Diode Forward Voltage	V_{SD}	I_S=1.0A,V_{GS}=0V I_S=-1.0A,V_{GS}=0V	N P			1.2 -1.2	V
Dynamic							
Total Gate Charge	Q_g	**N-Channel** V_{DS}=20V,V_{GS}=4.5V I_D≡12.0A **P-Channel** V_{DS}=-20V,V_{GS}=-4.5V I_D≡-12.0A	N P		5.5 9		nC
Gate-Source Charge	Q_{gs}		N P		1.25 2.54		
Gate-Drain Charge	Q_{gd}		N P		2.5 3.1		
Turn-On Time	$t_{d(on)}$ tr	**N-Channel** V_{DS}=20V,R_G=3.3Ω I_D=1A,V_{GS}=10V **P-Channel** V_{DS}=-20V,R_G=3.3Ω I_D=-1A,R_{GS}=-10V	N P		8.9 18.7		nS
			N P		2.2 12.7		
Turn-Off Time	$t_{d(off)}$ tf		N P		15.6 30.2		
			N P		3.0 15		

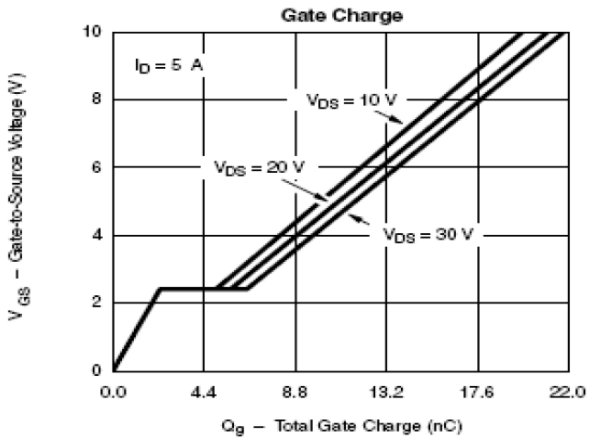
TYPICAL CHARACTERICTICS (N MOS)

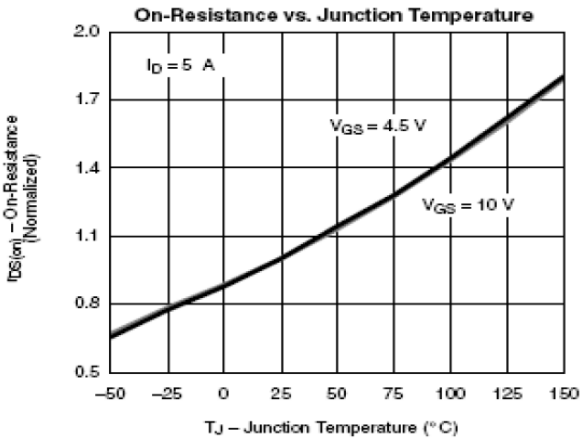






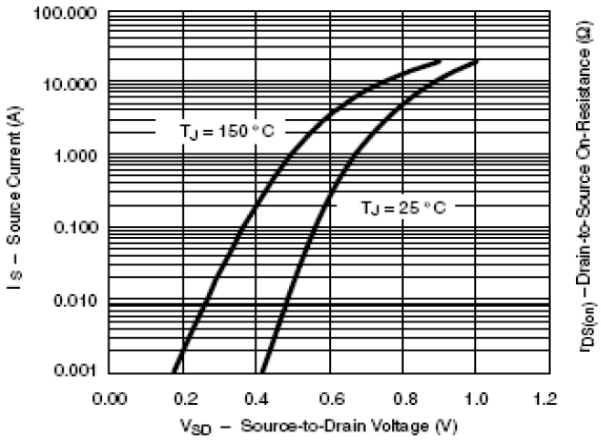




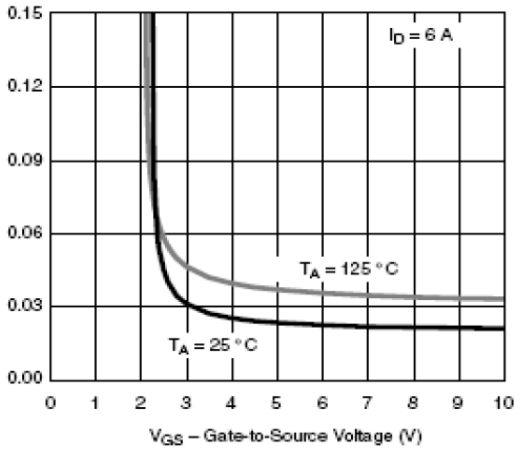


TYPICAL CHARACTERICTICS (N MOS)

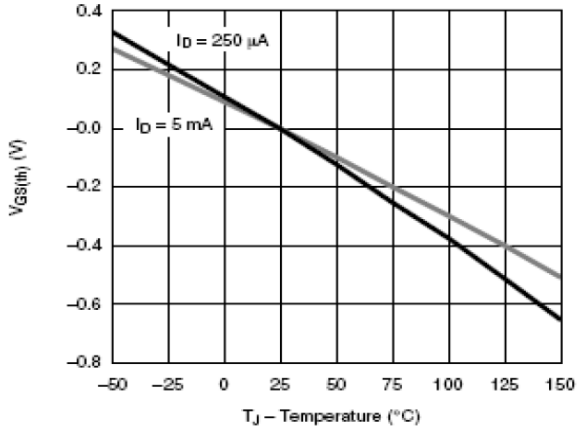
Source-Drain Diode Forward Voltage



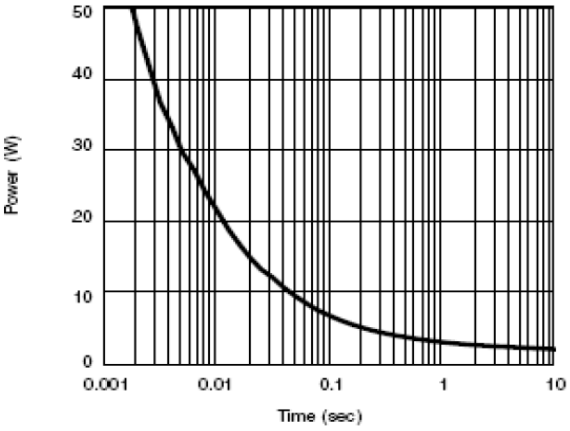
On-Resistance vs. Gate-to-Source Voltage



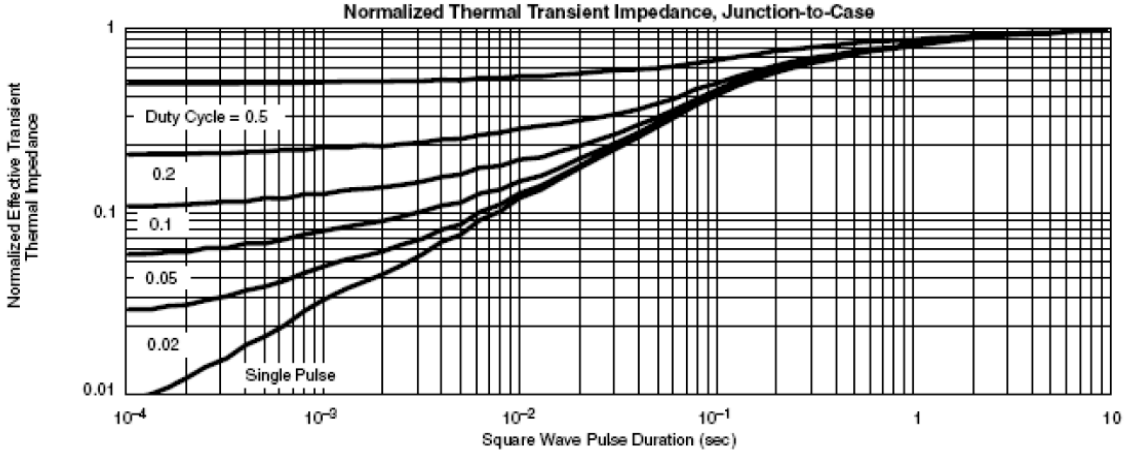
Threshold Voltage



Single Pulse Power, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case



YPICAL CHARACTERICTICS (P MOS)

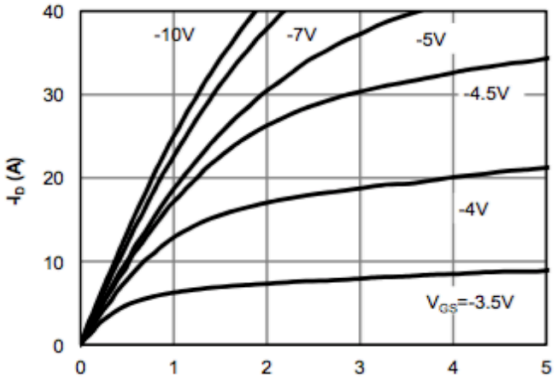


Fig 1: On-Region Characteristics (Note E)

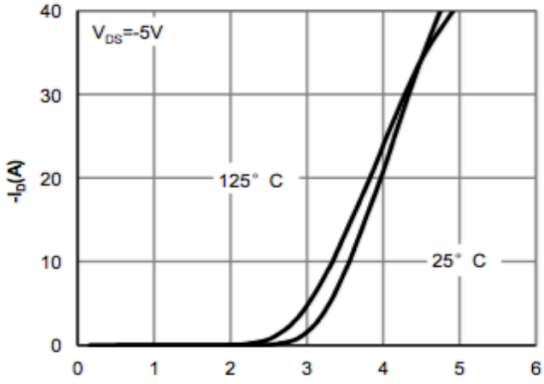


Figure 2: Transfer Characteristics (Note E)

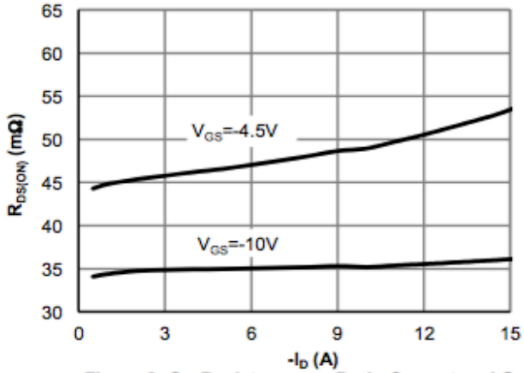


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

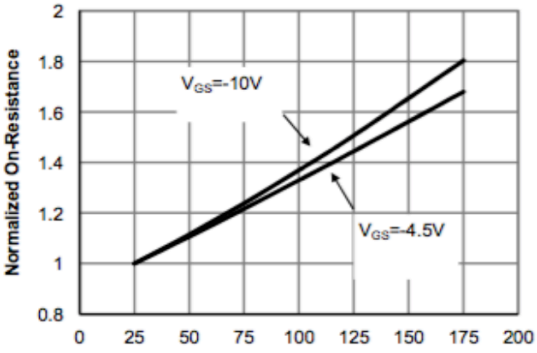


Figure 4: On-Resistance vs. Junction Temperature (Note E)

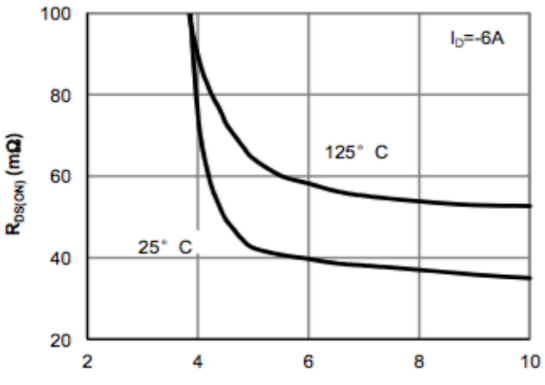


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

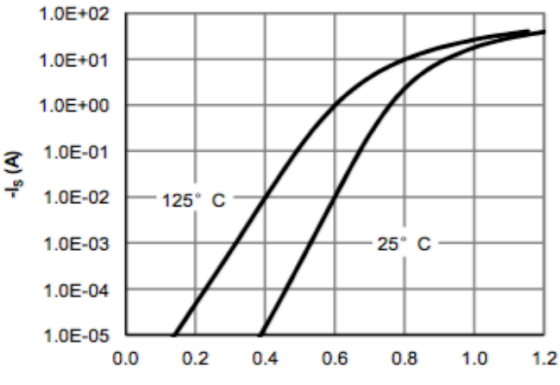


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL CHARACTERICTICS (P MOS)

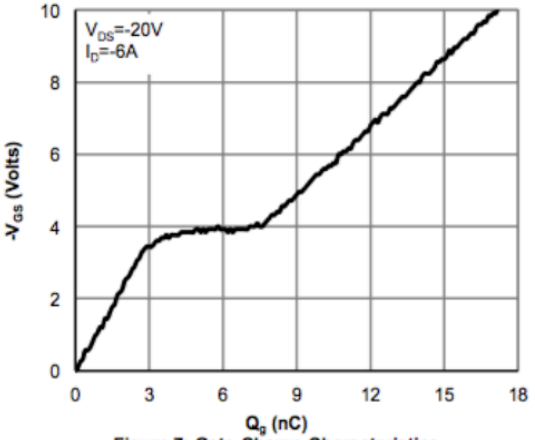


Figure 7: Gate-Charge Characteristics

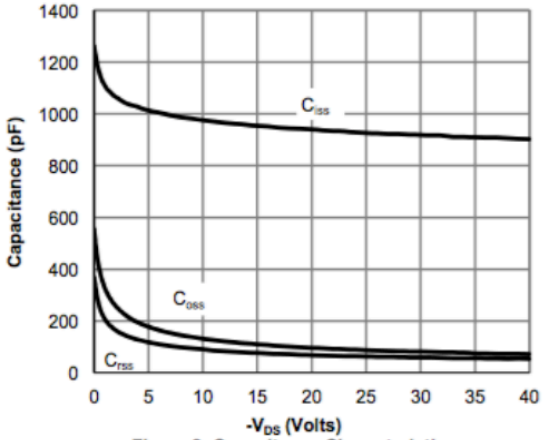


Figure 8: Capacitance Characteristics

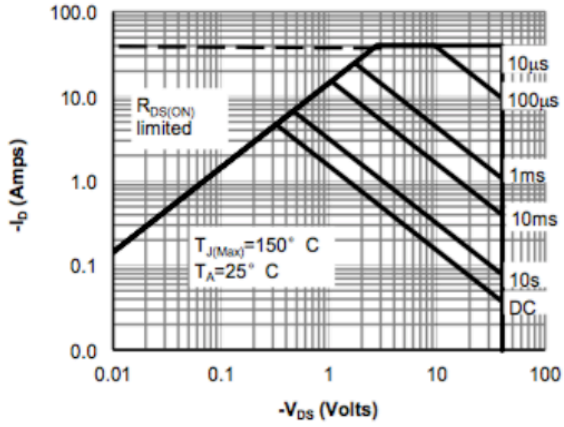


Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

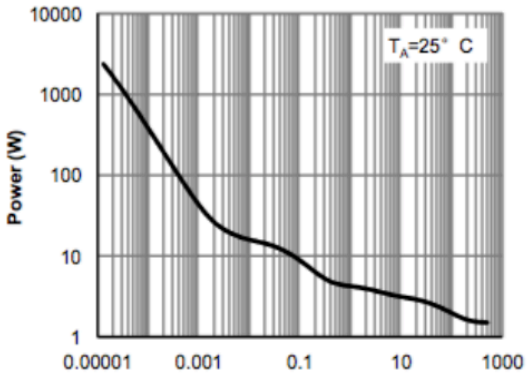


Figure 11: Single Pulse Power Rating Junction-to Ambient (Note F)

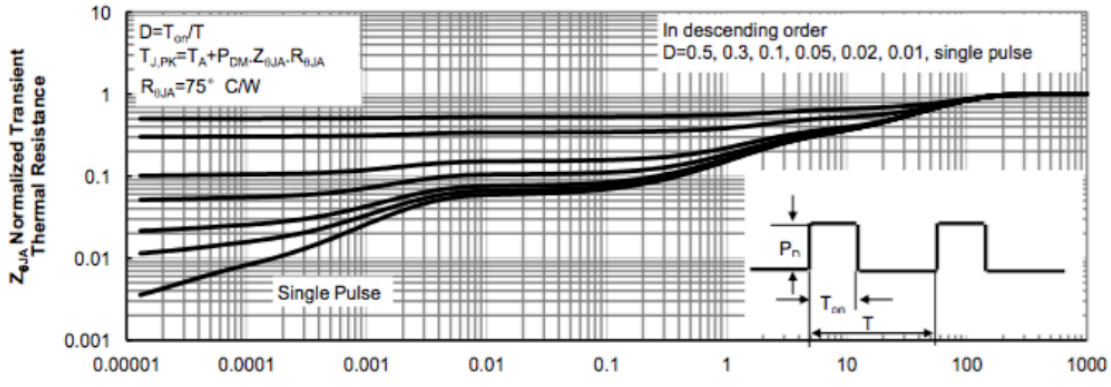


Figure 12: Normalized Maximum Transient Thermal Impedance (Note F)

TO252-4L PACKAGE OUTLINE