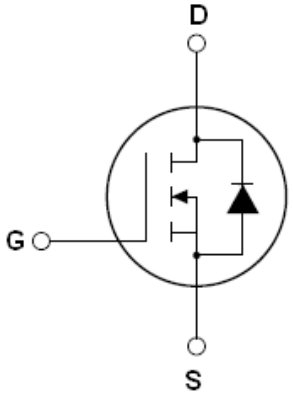
N-Channel Super Junction Power MOSFET

General Description

The series of devices use advanced super junction technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This super junction MOSFET fits the industry's AC-DC SMPS requirements for PFC, AC/DC power conversion, and industrial power applications.

V_{DS}	700	V
$R_{DS(ON)\ TYP.}$	165	mΩ
I_D	21	A



Schematic diagram

Features

- ●New technology for high voltage device
- ●Low on-resistance and low conduction losses
- ●Small package
- ●Ultra Low Gate Charge cause lower driving requirements
- ●100% Avalanche Tested
- ●ROHS compliant

Application

- Power factor correction（PFC）
- Switched mode power supplies(SMPS)
- Uninterruptible Power Supply（UPS）

Package Marking And Ordering Information

Device	Device Package	Marking
HMS21N70A	TO-3P	HMS21N70A

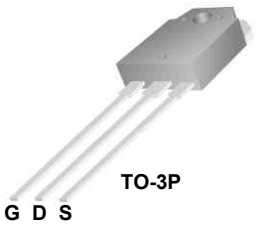


Table 1. Absolute Maximum Ratings (T_C=25℃)

Parameter	Symbol	NCE70R180T	Unit
Drain-Source Voltage (V_{GS}=0V）	V_{DS}	700	V
Gate-Source Voltage (V_{DS}=0V)	V_{GS}	±30	V
Continuous Drain Current at Tc=25°C	$I_{D\ (DC)}$	21	A
Continuous Drain Current at Tc=100°C	$I_{D\ (DC)}$	13.2	A
Pulsed drain current **(Note 1)**	$I_{DM\ (pluse)}$	63	A
Maximum Power Dissipation(Tc=25℃) Derate above 25°C	P_D	200 1.6	W W/°C
Single pulse avalanche energy **(Note 2)**	E_{AS}	690	mJ
Avalanche current **(Note 1)**	I_{AR}	7	A
Repetitive Avalanche energy ， t_{AR} limited by T_{jmax} **(Note 1)**	E_{AR}	1	mJ

Parameter	Symbol	NCE70R180T	Unit
Drain Source voltage slope, V_{DS} ≤480 V,	dv/dt	50	V/ns
Reverse diode dv/dt， V_{DS} ≤480 V,I_{SD}<I_D	dv/dt	15	V/ns
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55...+150	°C

* limited by maximum junction temperature

Table 2. Thermal Characteristic

Parameter	Symbol	NCE70R180T	Unit
Thermal Resistance，Junction-to-Case（Maximum）	R_{thJC}	0.62	°C /W
Thermal Resistance，Junction-to-Ambient （Maximum）	R_{thJA}	62.5	°C /W

Table 3. Electrical Characteristics (TA=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
On/off states						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	700			V
Zero Gate Voltage Drain Current(Tc=25℃)	I_{DSS}	V_{DS}=650V,V_{GS}=0V		0.05	1	μA
Zero Gate Voltage Drain Current(Tc=125℃)	I_{DSS}	V_{DS}=650V,V_{GS}=0V			100	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±30V,V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2.5	3	3.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=10.5A		165	190	mΩ
Dynamic Characteristics						
Forward Transconductance	g_{FS}	V_{DS} = 20V, I_D = 10.5A		17.5		S
Input Capacitance	C_{lss}	V_{DS}=50V,V_{GS}=0V, F=1.0MHz		1950		PF
Output Capacitance	C_{oss}			150		PF
Reverse Transfer Capacitance	C_{rss}			5		PF
Total Gate Charge	Q_g	V_{DS}=480V,I_D=21A, V_{GS}=10V		45	70	nC
Gate-Source Charge	Q_{gs}			9		nC
Gate-Drain Charge	Q_{gd}			18		nC
Intrinsic gate resistance	R_G	f = 1 MHz open drain		1		Ω
Switching times						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=380V,I_D=11A, R_G=4Ω,V_{GS}=10V		11		nS
Turn-on Rise Time	t_r			6		nS
Turn-Off Delay Time	$t_{d(off)}$			61	100	nS
Turn-Off Fall Time	t_f			4.5	12	nS
Source- Drain Diode Characteristics						
Source-drain current(Body Diode)	I_{SD}	T_C=25°C			21	A
Pulsed Source-drain current(Body Diode)	I_{SDM}				63	A
Forward on voltage	V_{SD}	Tj=25°C,I_{SD}=21A,V_{GS}=0V		0.9	1.3	V
Reverse Recovery Time	t_{rr}	Tj=25°C,I_F=21A,di/dt=100A/μs		310		nS
Reverse Recovery Charge	Q_{rr}			5		uC
Peak Reverse Recovery Current	I_{rrm}			28		A

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2. Tj=25℃,VDD=50V,VG=10V, R_G=25Ω

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (curves)

Figure1. Safe operating area

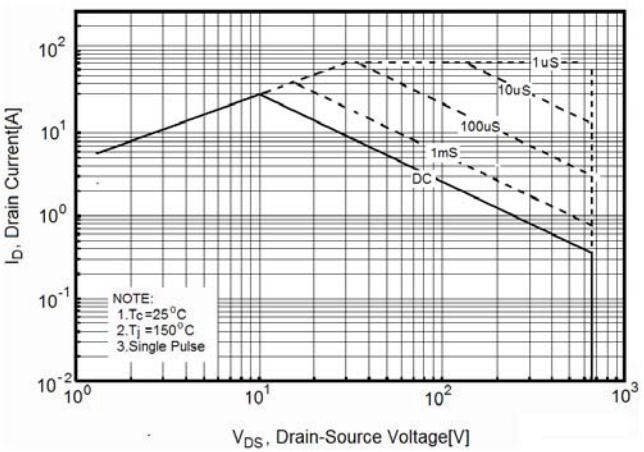


Figure3. Source-Drain Diode Forward Voltage

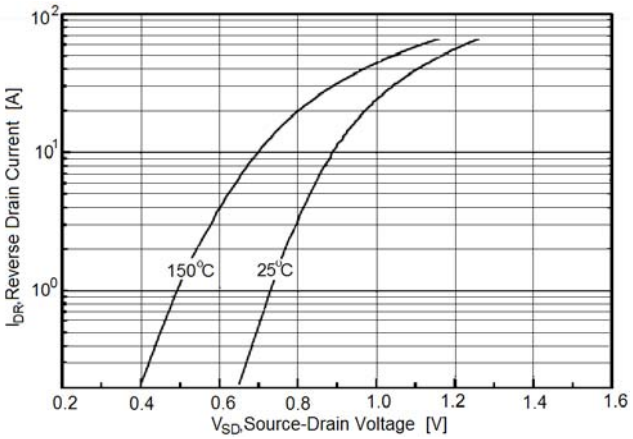


Figure4. Output characteristics

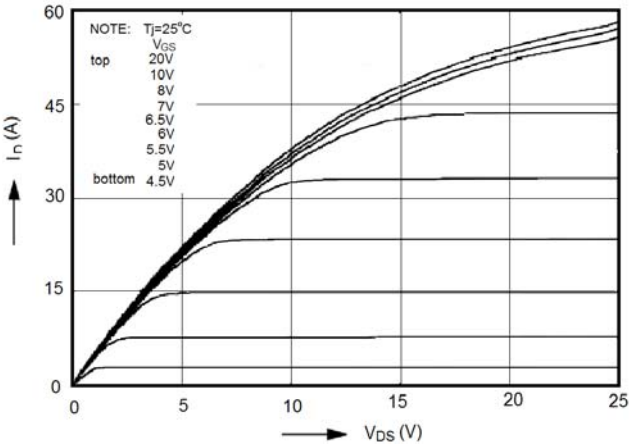


Figure5. Transfer characteristics

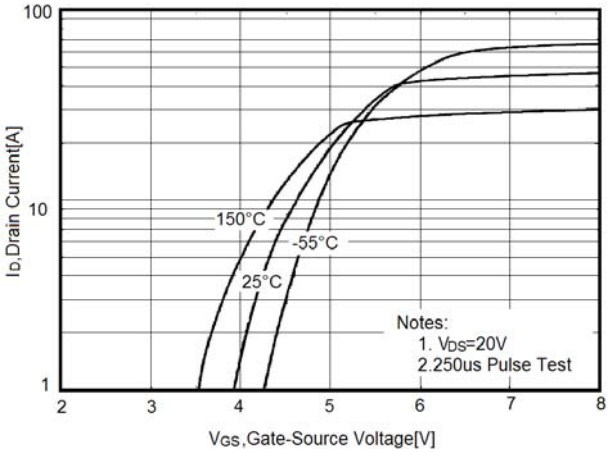


Figure6. Static drain-source on resistance

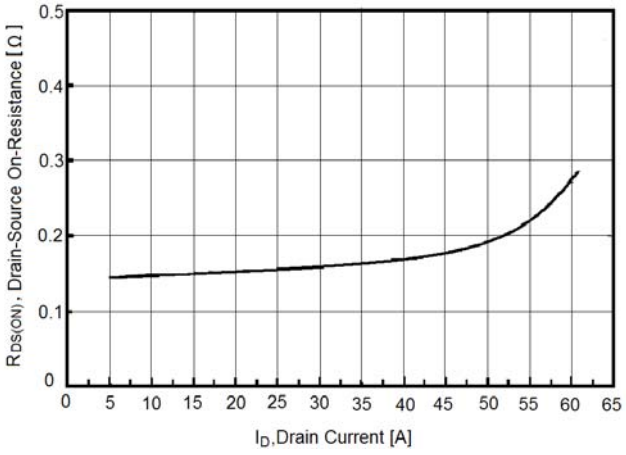


Figure7. $R_{DS(ON)}$ vs Junction Temperature

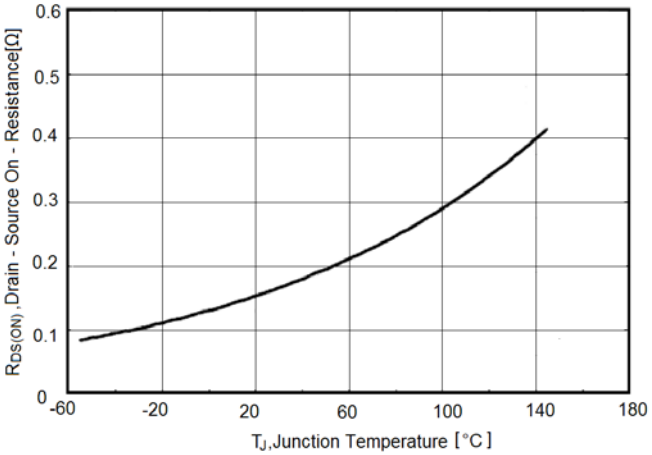


Figure8. BV_{DSS} vs Junction Temperature

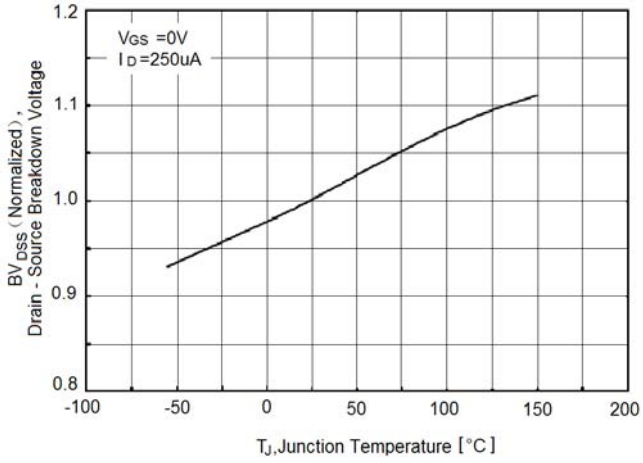


Figure9. Maximum I_D vs Junction Temperature

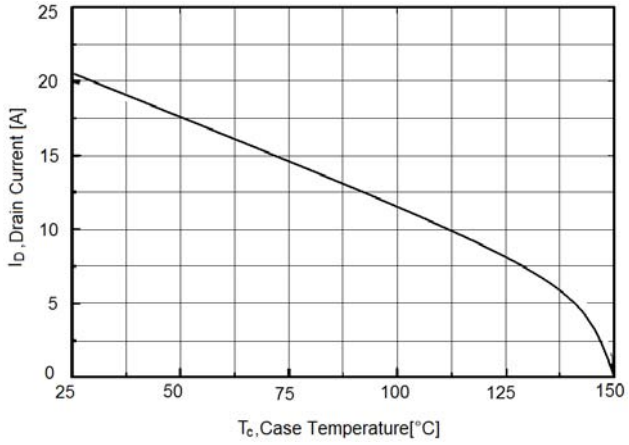


Figure10. Gate charge waveforms

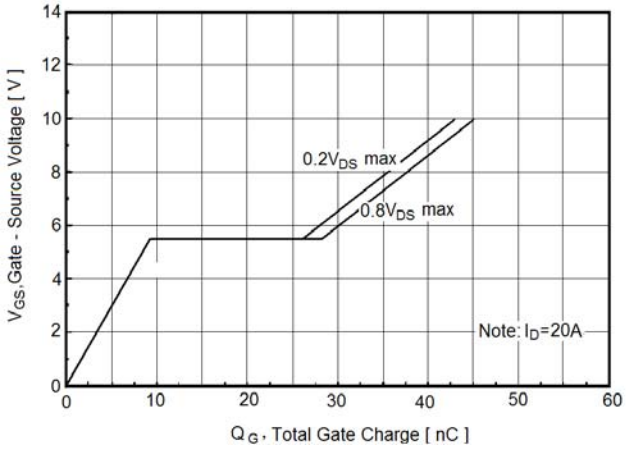


Figure11. Capacitance

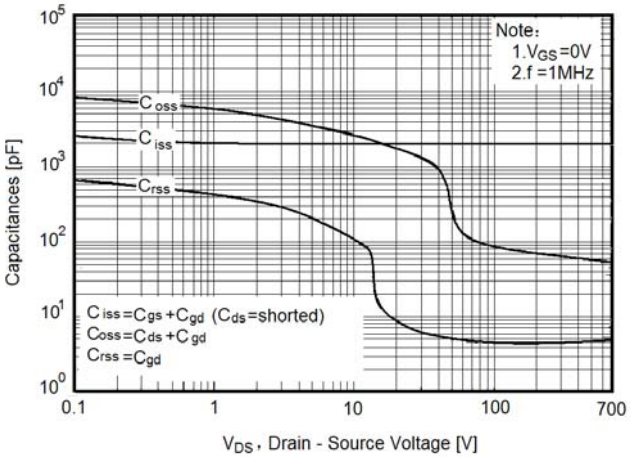
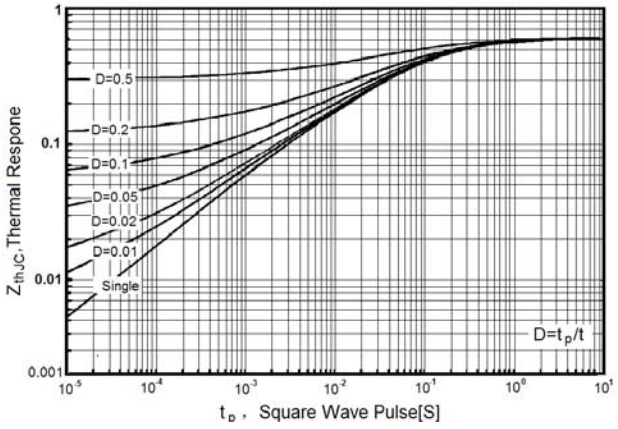
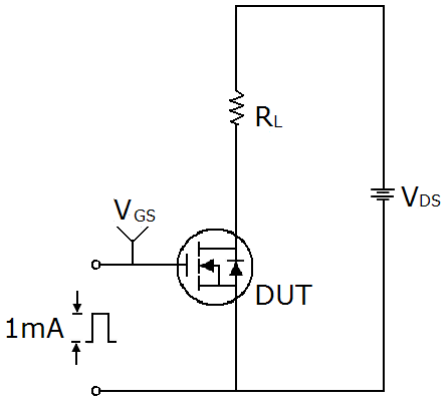


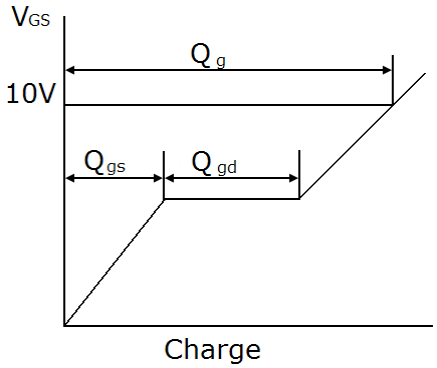
Figure12. Transient Thermal Impedance



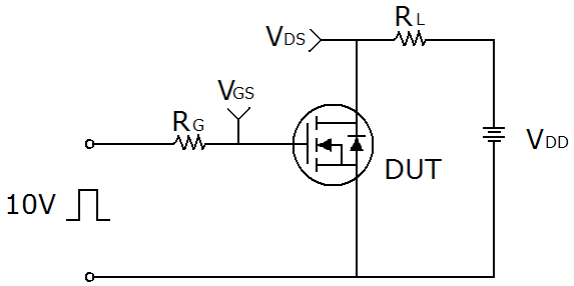
Test circuit

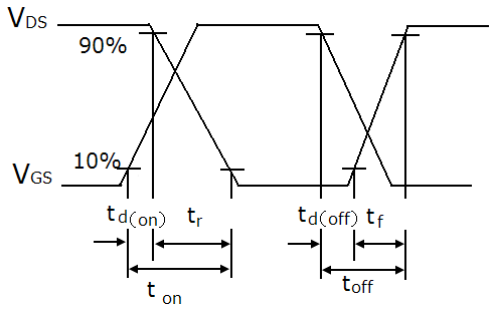
1）Gate charge test circuit & Waveform



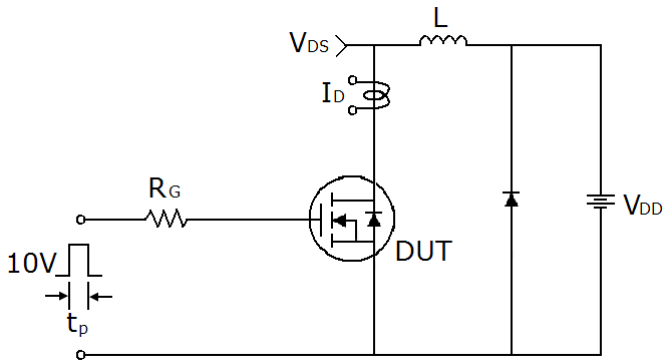


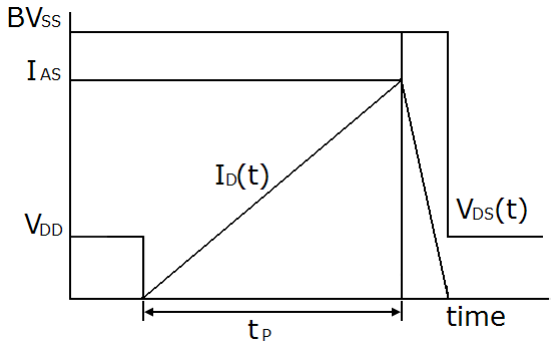
2）Switch Time Test Circuit：





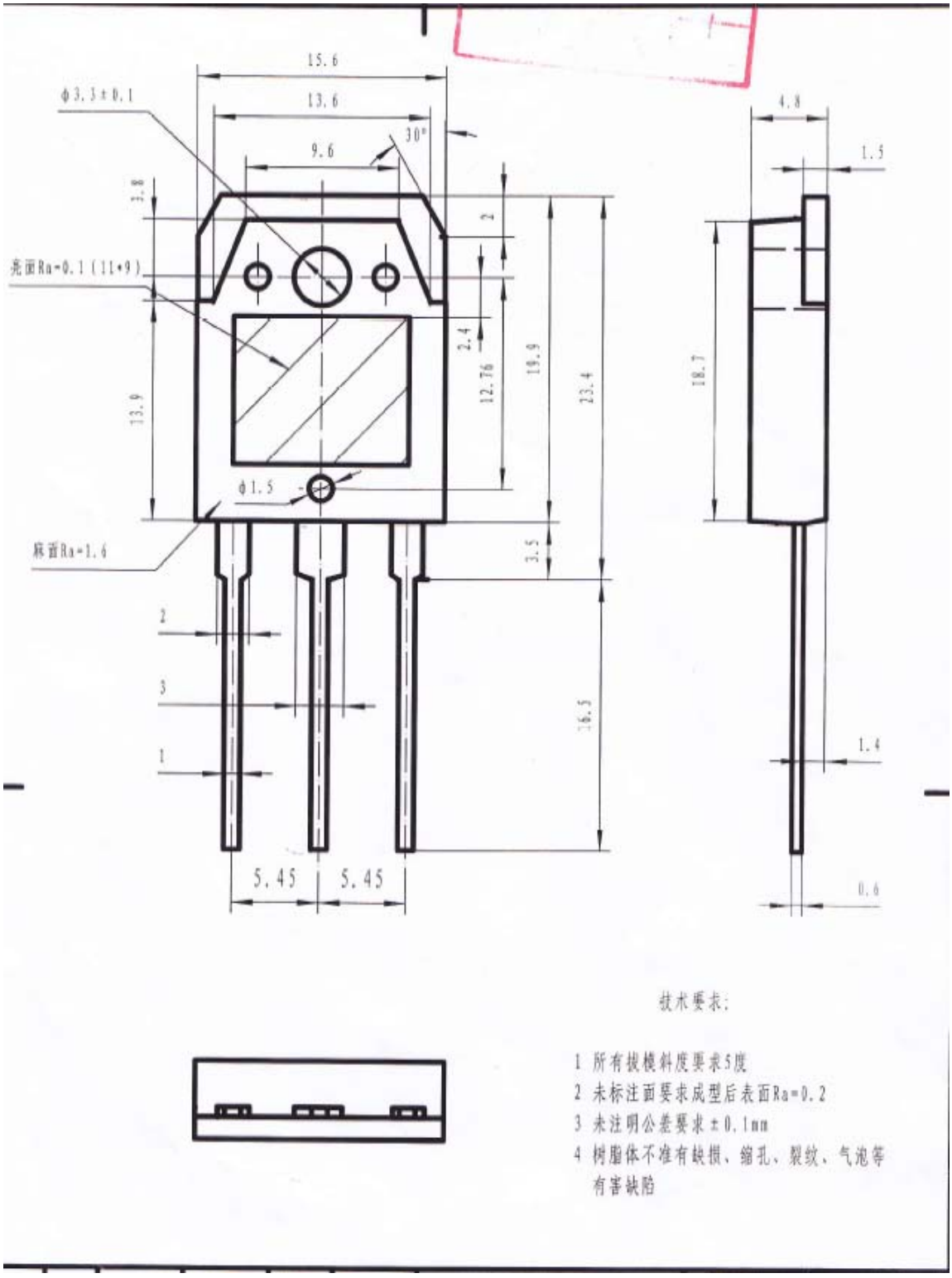
3）Unclamped Inductive Switching Test Circuit & Waveforms





Package Dimensions

TO-3P



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