

## P-Channel Enhancement Mode Power MOSFET

### Description

The HM4421 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge .This device is well suited for high current load applications.

### General Features

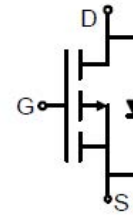
- $V_{DS} = -60V, I_D = -12.5A$   
 $R_{DS(ON)} < 28m\Omega @ V_{GS} = -10V$
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation

### Application

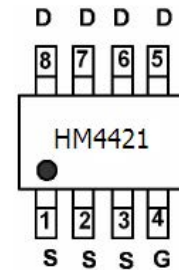
- Load switch

**100% UIS TESTED!**

**100%  $\Delta V_{ds}$  TESTED!**



Schematic diagram



Marking and pin Assignment



SOP-8 top view

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM4421	HM4421	SOP8	-	-	-

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	-12.5	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D (100^\circ C)$	-9	A
Pulsed Drain Current	$I_{DM}$	-36	A
Maximum Power Dissipation	$P_D$	95	W
Derating factor		0.76	W/ $^\circ C$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	722	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ C$

### Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	1.31	$^\circ C/W$
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**Electrical Characteristics ( $T_c=25^{\circ}\text{C}$  unless otherwise noted)**

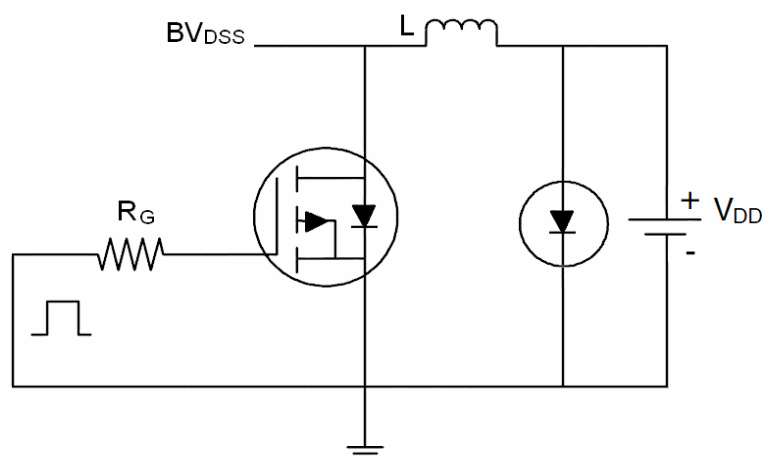
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =-250μA	-60	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-60V, V <sub>GS</sub> =0V	-	-	-1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.2	-1.9	-2.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-10A	-	23	28	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =-10V, I <sub>D</sub> =-10A	-	25	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-25V, V <sub>GS</sub> =0V, F=1.0MHz	-	6460	-	PF
Output Capacitance	C <sub>oss</sub>		-	719	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	535	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =-30V, R <sub>L</sub> =1.5Ω, V <sub>GS</sub> =-10V, R <sub>G</sub> =3Ω	-	15	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	17	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	40	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	45	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-30, I <sub>D</sub> =-10A, V <sub>GS</sub> =-10V	-	75		nC
Gate-Source Charge	Q <sub>gs</sub>		-	16		nC
Gate-Drain Charge	Q <sub>gd</sub>		-	19		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =-10A	-		-1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	-20	A
Reverse Recovery Time	t <sub>rr</sub>	TJ = 25°C, IF =- 10A	-	50		nS
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = -100A/μs(Note3)	-	59		nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

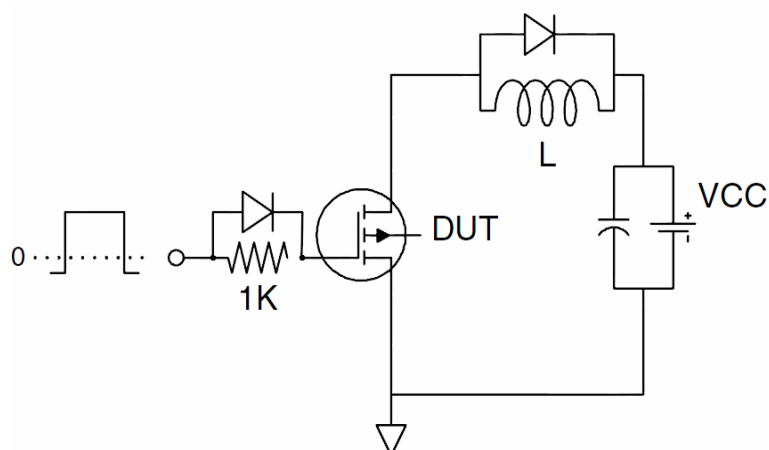
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5.  $E_{AS}$  condition:  $T_J=25^{\circ}\text{C}, V_{DD}=-20V, V_G=-10V, L=1mH, R_g=25\Omega, I_{AS}=38A$

## Test Circuit

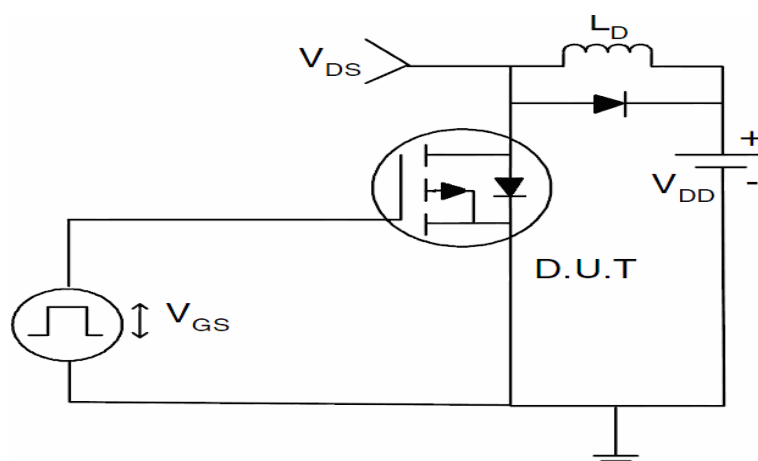
### 1) $E_{AS}$ Test Circuit



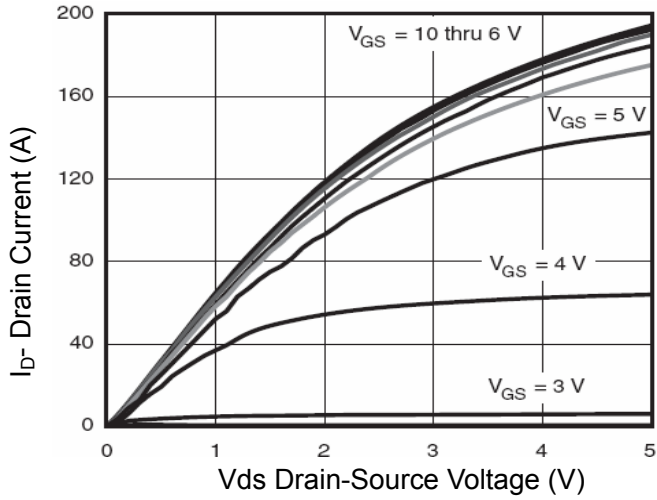
### 2) Gate Charge Test Circuit



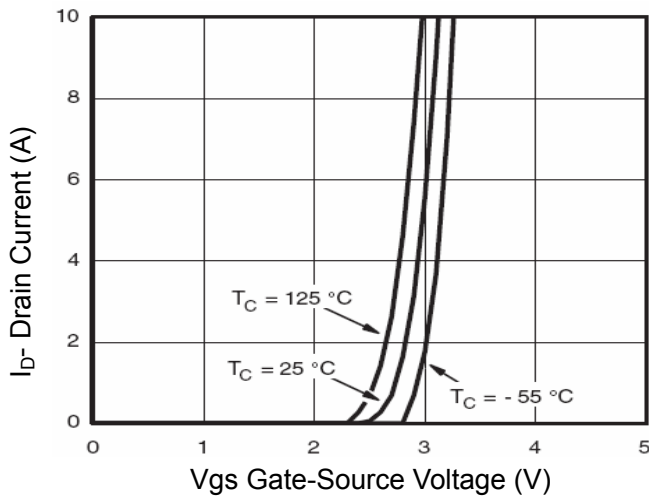
### 3) Switch Time Test Circuit



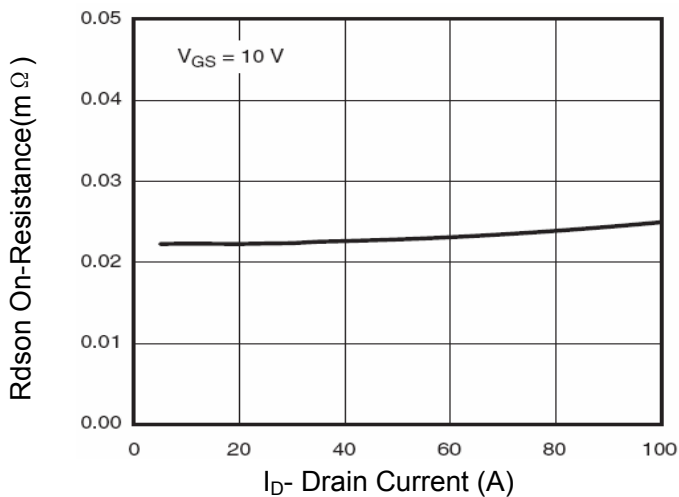
**Typical Electrical and Thermal Characteristics (Curves)**



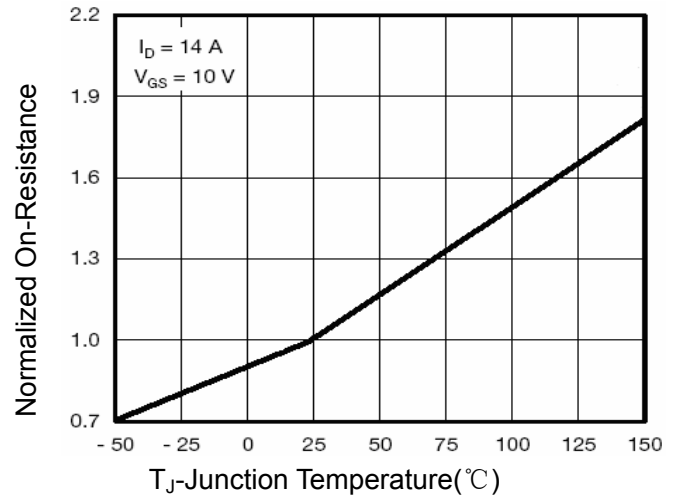
**Figure 1 Output Characteristics**



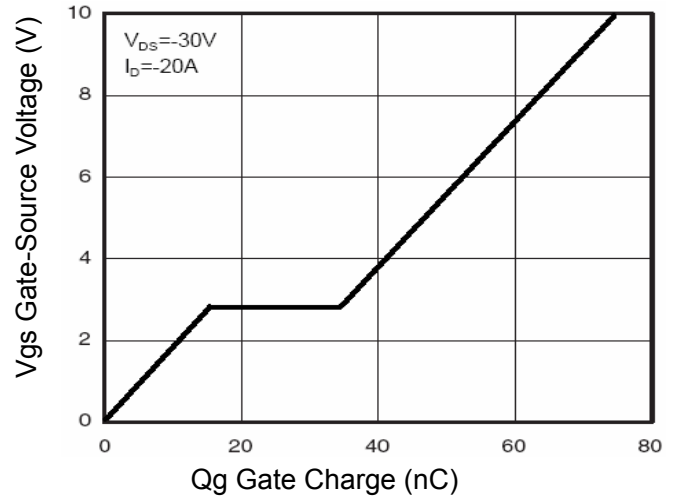
**Figure 2 Transfer Characteristics**



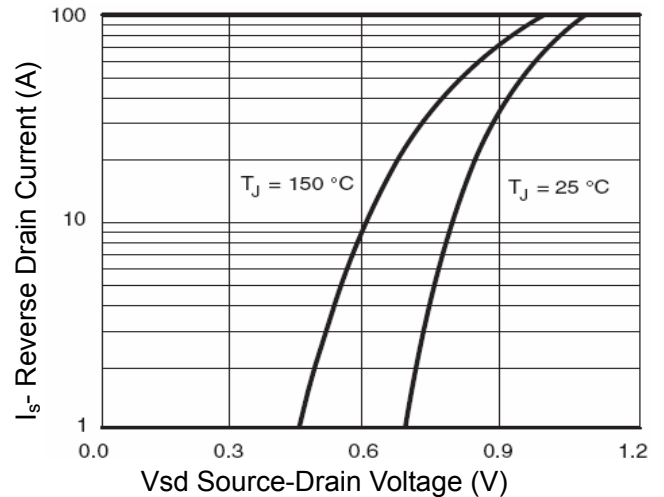
**Figure 3 Rdson- Drain Current**



**Figure 4 Rdson-Junction Temperature**



**Figure 5 Gate Charge**



**Figure 6 Source- Drain Diode Forward**

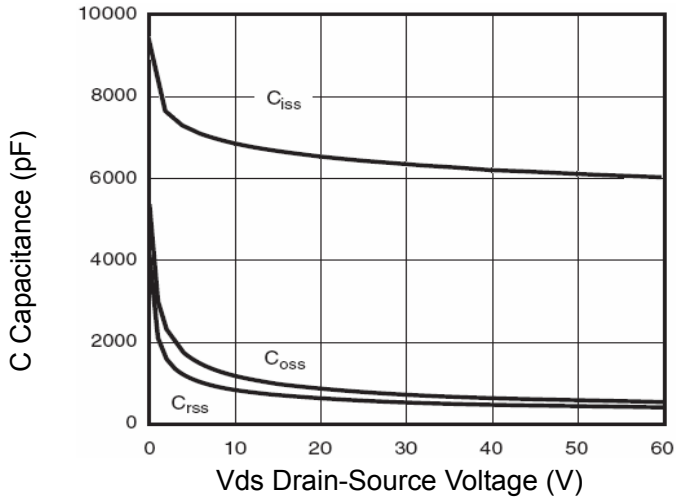


Figure 7 Capacitance vs Vds

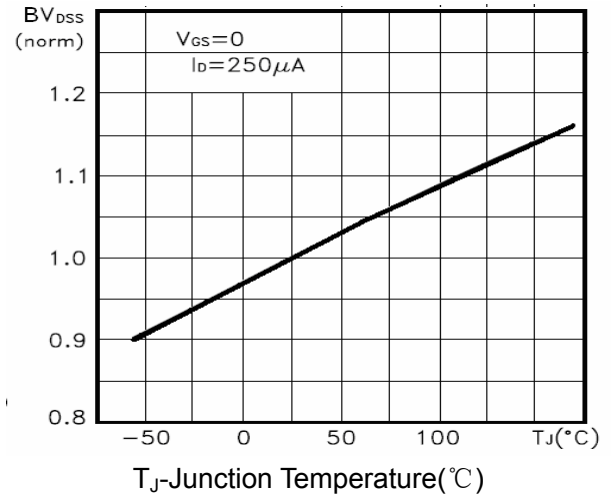


Figure 9  $BV_{DSS}$  vs Junction Temperature

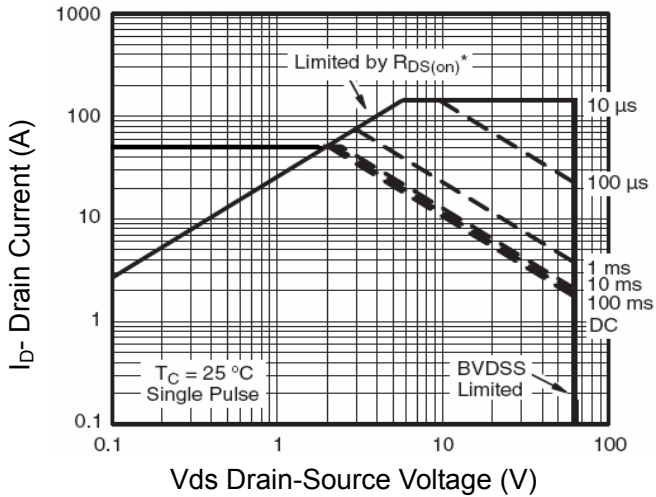


Figure 8 Safe Operation Area

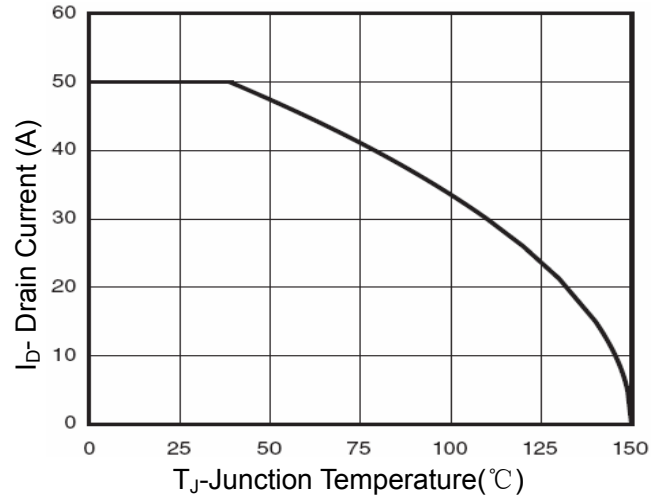


Figure 10  $I_D$  Current Derating vs Junction Temperature

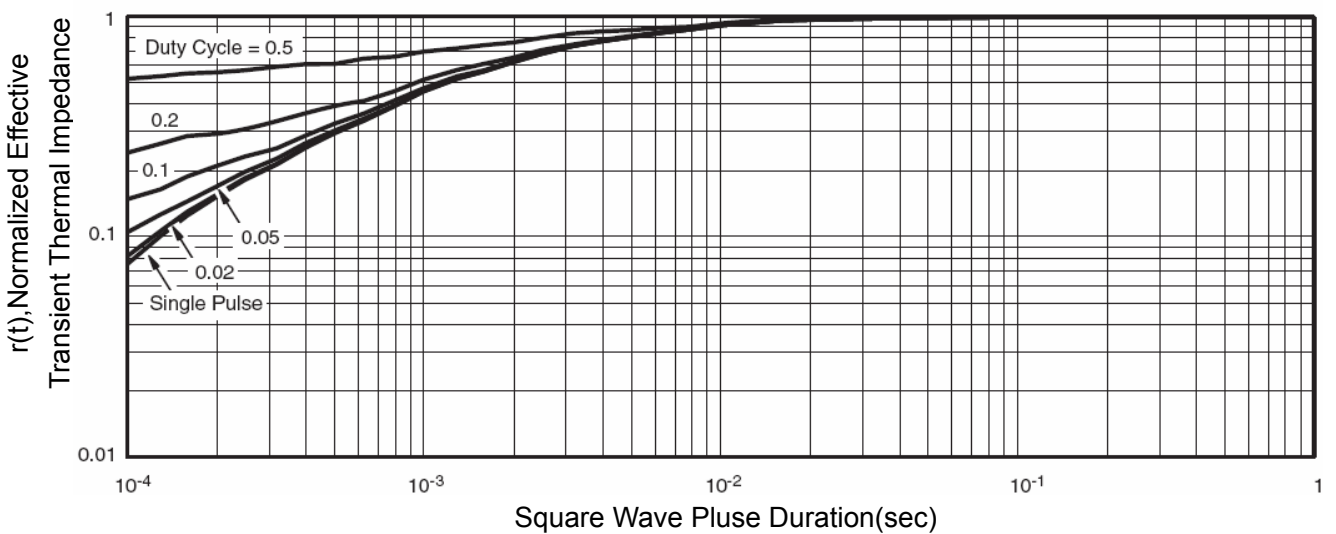
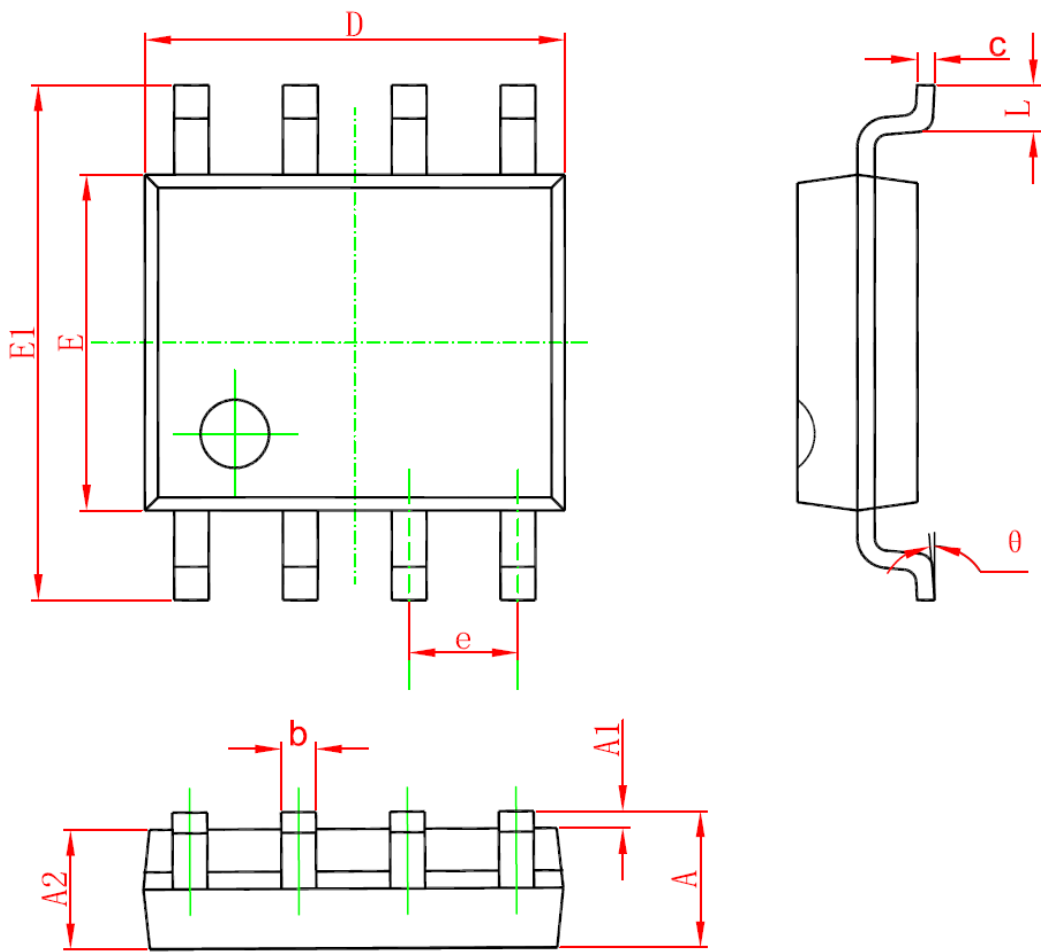


Figure 11 Normalized Maximum Transient Thermal Impedance

SOP-8 PACKAGE IN FORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
$\theta$	0°	8°	0°	8°

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