

N-Channel Super Trench Power MOSFET

Description

The HMS80N15D uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

General Features

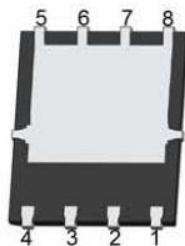
- $V_{DS} = 150V, I_D = 80A$
 $R_{DS(ON)} = 10.0m\Omega$ (typical) @ $V_{GS} = 10V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating

100% UIS TESTED!
100% ΔV_{ds} TESTED!

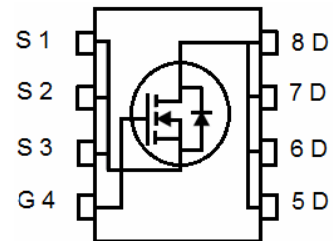
DFN 5X6



Top View



Bottom View



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HMS80N15D	HMS80N15D	DFN5X6-8L	-	-	-

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	150	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	80	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	52	A
Pulsed Drain Current	I_{DM}	320	A
Maximum Power Dissipation	P_D	160	W
Derating factor		1.28	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	550	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.78	$^\circ C/W$
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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	150	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =150V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	2.0		4.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =40A	-	10	11.5	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V,I _D =40A	-	58	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =75V,V _{GS} =0V, F=1.0MHz	-	2200	2700	PF
Output Capacitance	C _{oss}		-	289	450	PF
Reverse Transfer Capacitance	C _{rss}		-	11.2	18	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =75V, I _D =40A V _{GS} =10V,R _G =3Ω	-	12.5	-	nS
Turn-on Rise Time	t _r		-	3.8	-	nS
Turn-Off Delay Time	t _{d(off)}		-	14	-	nS
Turn-Off Fall Time	t _f		-	3.5	-	nS
Total Gate Charge	Q _g	V _{DS} =75V,I _D =40A, V _{GS} =10V	-	33	40	nC
Gate-Source Charge	Q _{gs}		-	14.5	18	nC
Gate-Drain Charge	Q _{gd}		-	8	10	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V,I _S =40A	-	-	1.2	V
Diode Forward Current (Note 2)	I _S		-	-	80	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 40A	-	47	-	nS
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs (Note3)	-	55	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^{\circ}\text{C}$. the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. E_{AS} condition : $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

Typical Electrical and Thermal Characteristics

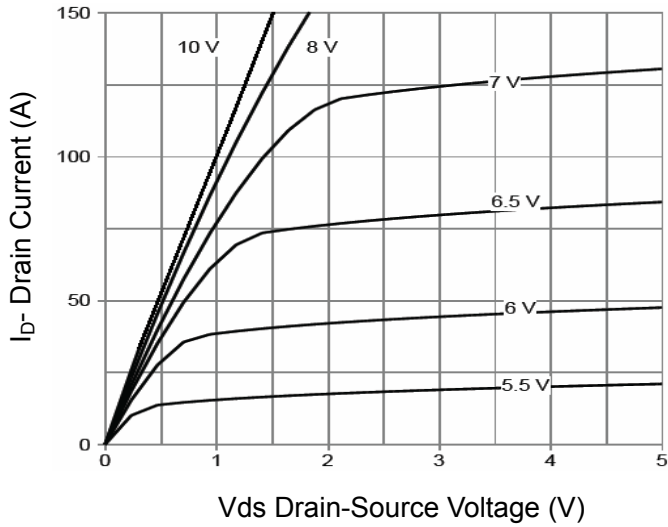


Figure 1 Output Characteristics

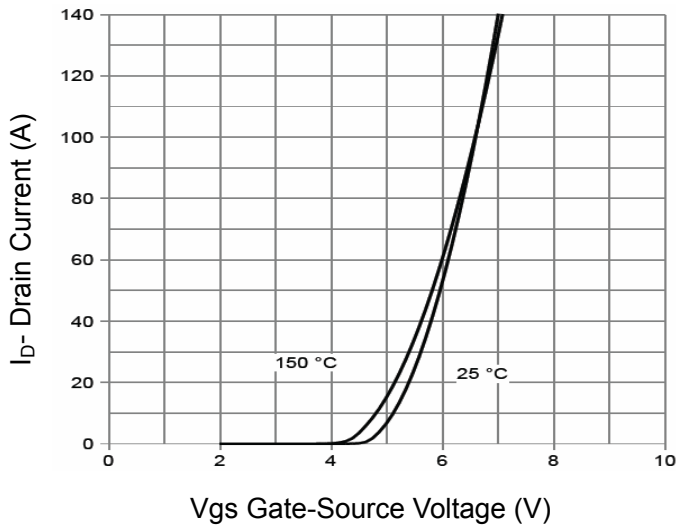


Figure 2 Transfer Characteristics

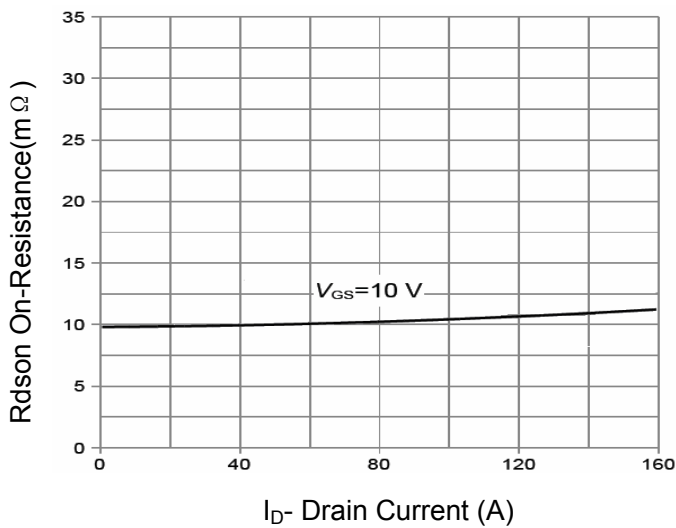


Figure 3 $R_{DS(on)}$ - Drain Current

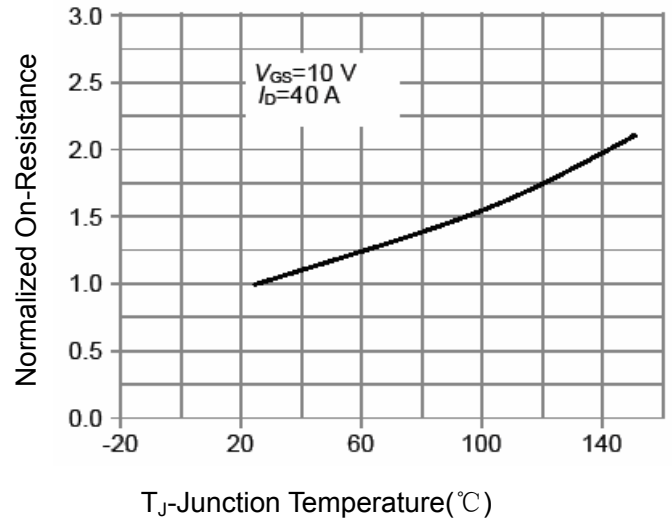


Figure 4 $R_{DS(on)}$ -Junction Temperature

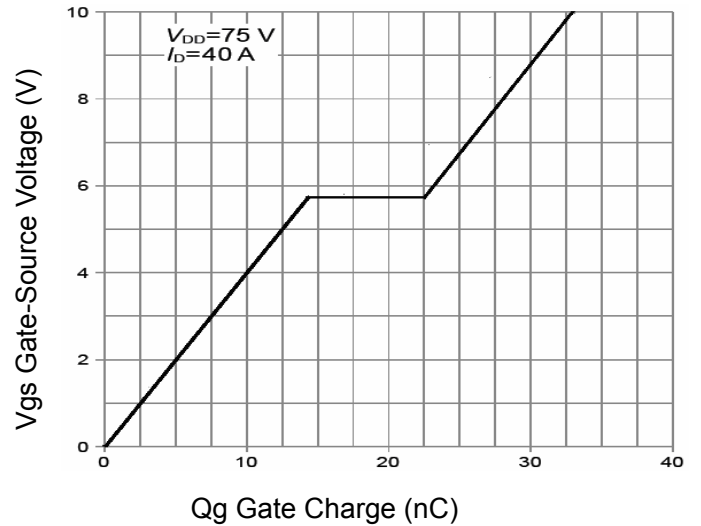


Figure 5 Gate Charge

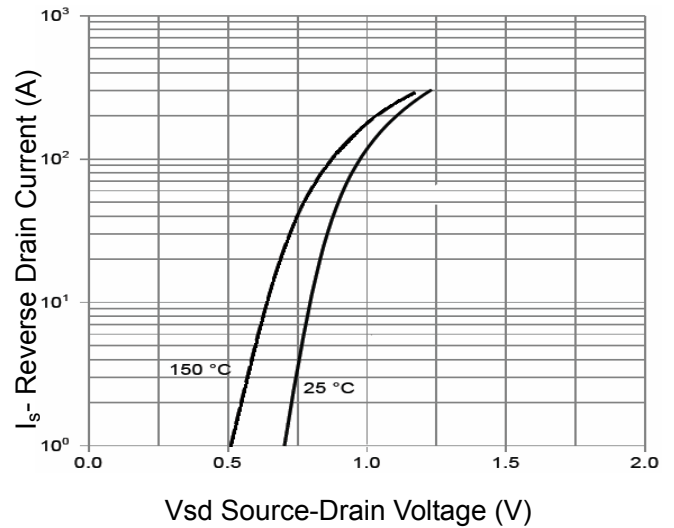


Figure 6 Source- Drain Diode Forward

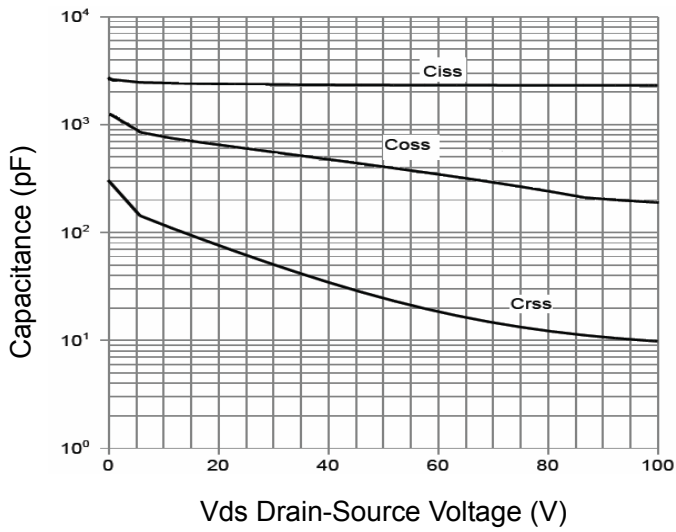


Figure 7 Capacitance vs Vds

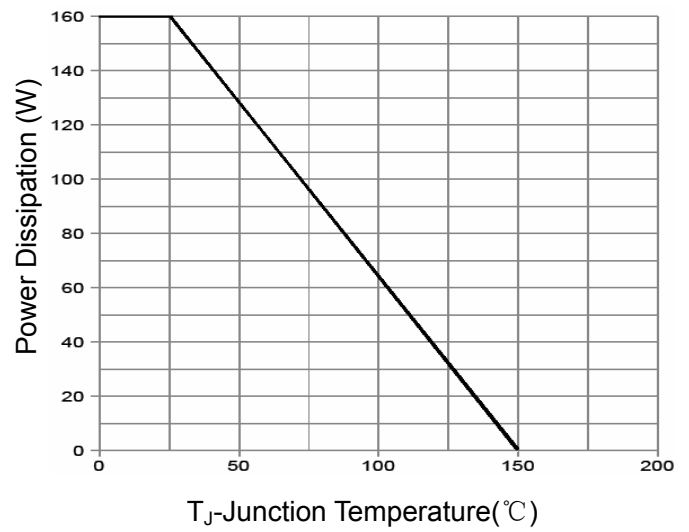


Figure 9 Power De-rating

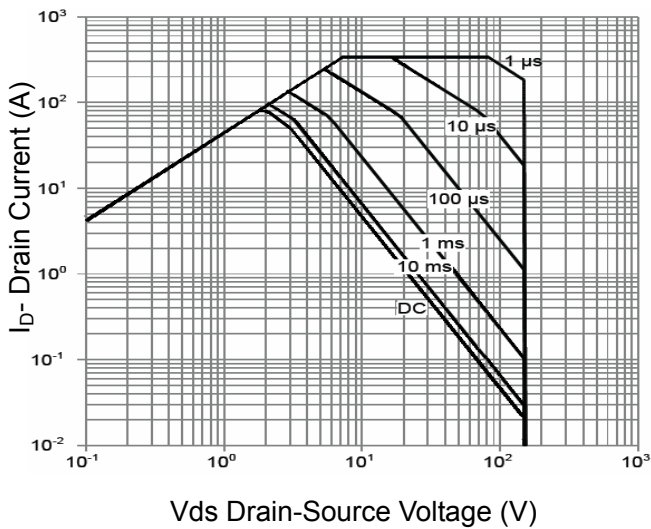


Figure 8 Safe Operation Area

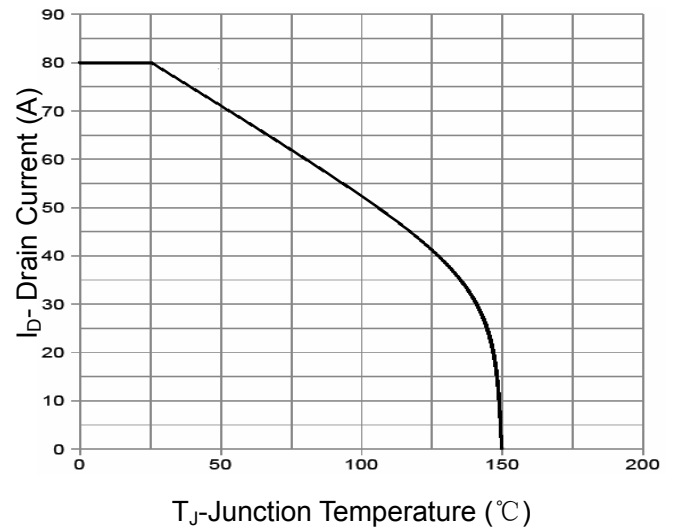


Figure 10 Current De-rating

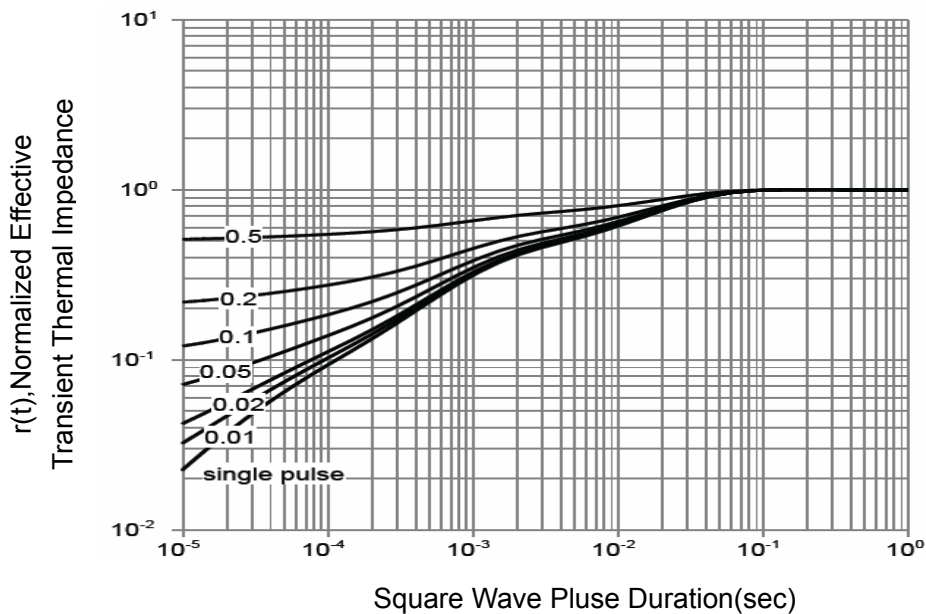


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package Information

