

Standoff 42V 0.6A 800kHz Sync Step-Down Regulator

Features

- Wide 4V to 38V Operating Input Range
- Standoff Voltage: 42V
- 600mA Continuous Output Current
- Fixed 800kHz Switching Frequency
- Built-in Over Current Limit
- Built-in Over Voltage Protection
- Non-A option Support PSM Mode
- A option Support Force-PWM Mode
- Low Shutdown I_Q : <10- μ A Typical
- Internal Soft-Start
- High Efficiency at 12V-3.3V: Up to 90%
- 500m Ω /300m Ω Low $R_{DS(ON)}$ Internal Power MOSFETs
- Output Adjustable from 0.8V
- No Schottky Diode Required
- Short Protection with Hiccup-Mode
- Integrated internal compensation
- Thermal Shutdown
- -40 °C to +85 °C Temperature Range
- Available in SOT23-6 Package

Applications

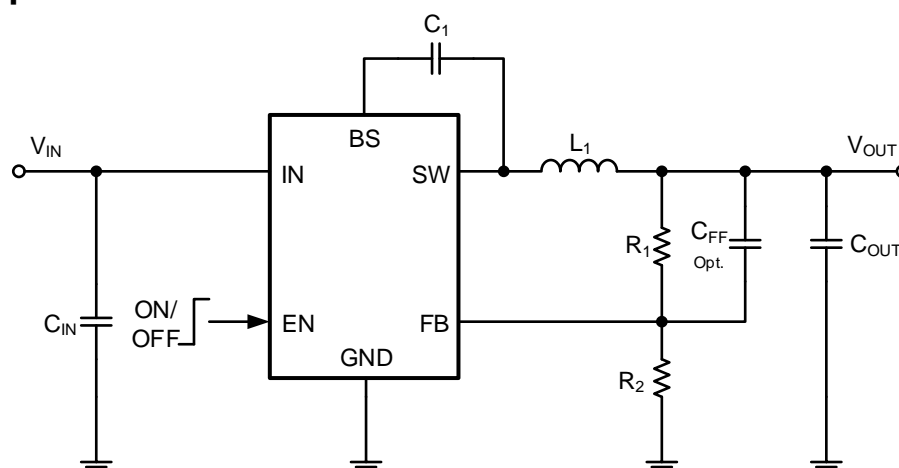
- Battery-Powered Equipment
- Portable Media Players
- Industrial Distributed Power Applications
- Portable Hand-Held Instruments

General Description

The J O : 338 devices are high-efficiency, synchronous step-down DC/DC regulators. With a wide input range, they are suitable for a wide range of applications, such as power conditioning from unregulated sources. They feature a low $R_{DS(ON)}$ (500m Ω /300m Ω typical) internal switch for maximum efficiency (92% typical). Support PSM mode (Non-A Option) and Force-PWM mode (A option), Operating frequency is fixed at 800kHz, allowing the use of small external components while still being able to have low output voltage ripple. With OVP function, the IC can stand off input voltage as high as 45V. The J O : 338 support 600mA Continuous Output Current, they all have a 0.8V nominal feedback voltage.

Additional features include: thermal shutdown, V_{IN} undervoltage lockout, and gate drive undervoltage lockout. The J O : 338 are available in a low-profile SOT23-6 package.

Typical Application Circuit

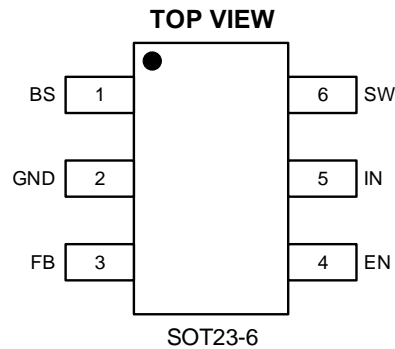


Basic Application Circuit

Standoff 42V 0.6A 800kHz Sync Step-Down Regulator

Pin Description

Pin Configuration



J O : 338 Top Marking: HAYLL (device code: HA, Y=year code, LL= lot number code)

Pin Description

Pin	Name	Function
1	BS	Bootstrap. A capacitor connected between SW and BS pins is required to form a floating supply across the high-side switch driver.
2	GND	Ground Pin
3	FB	Adjustable Version Feedback input. Connect FB to the center point of the external resistor divider
4	EN	Drive this pin to a logic-high to enable the IC. Drive to a logic-low to disable the IC and enter micro-power shutdown mode.
5	IN	Power Supply Pin
6	SW	Switching Pin, Connect to inductor, diode, and BS capacitor.

Order Information

Marking	Part No.	Model	Description	Package	T/R
HAYLL	"70301600 ""	J O : 338	J O : 338 PSM SYN Buck, 4-42V, 600mA, 800kHz, VFB 0.8V, SOT23-6	SOT236	3000PCS

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Specifications

Absolute Maximum Ratings ^{(1) (2)}

Item	Min	Max	Unit
V _{IN} voltage	-0.3	42	V
EN voltage	-0.3 (V _{IN} + 0.3 V)	42	V
SW voltage	-0.3	42	V
BS voltage above SW voltage		7	V
FB voltage	-0.3	42	V
Power dissipation ⁽³⁾	Internally Limited		
Maximum junction temperature		150	℃
Storage temperature, T _{stg}	-65	150	℃

Note (1): Exceeding these ratings may damage the device.

Note (2): The device is not guaranteed to function outside of its operating conditions.

Note (3): The maximum allowable power dissipation is a function of the maximum junction temperature, T_{J(MAX)}, the junction-to-ambient thermal resistance, R_{θJA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: P_{D(MAX)} = (T_{J(MAX)} - T_A)/R_{θJA}. Exceeding the maximum allowable power dissipation causes excessive die temperature, and the regulator goes into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=175 ℃ (typical) and disengages at T_J= 155 ℃ (typical).

ESD Ratings

Item	Description	Value	Unit
V _(ESD-HBM)	Human Body Model (HBM) ANSI/ESDA/JEDEC JS-001-2014 Classification, Class: 2	±2000	V
V _(ESD-CDM)	Charged Device Mode (CDM) ANSI/ESDA/JEDEC JS-002-2014 Classification, Class: C0b	±200	V
I _{LATCH-UP}	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	±150	mA

Recommended Operating Conditions

Item	Min	Max	Unit
Operating junction temperature ⁽¹⁾	-40	125	℃
Input voltage V _{IN}	4	38	V
SW voltage		38	V

Note (1): All limits specified at room temperature (T_A = 25 ℃) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

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Thermal Information

Item	Description	Value	Unit
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾⁽²⁾	120	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	90	°C/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.

Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board

Electrical Characteristics ^{(1) (2) (3)}

Note (1): V_{IN}=12V, T_A = 25 °C, unless otherwise noted.

Parameter	Test Conditions	Min	Typ.	Max	Unit
Input Voltage Range		4		38	V
Supply Current in Operation	PSM Mode		400	800	uA
	PWM Mode		5	10	mA
Supply Current in Shutdown	V _{EN} =0 or EN = GND			10	uA
Regulated Feedback Voltage		0.785	0.800	0.815	V
High-Side Switch On-Resistance			500		mΩ
Low-Side Switch On-Resistance			300		mΩ
High-Side Switch Leakage Current	V _{EN} =0V, V _{SW} =0V			1	uA
Upper Switch Current Limit	Minimum Duty Cycle	1			A
Switching Frequency			800		kHz
Maximum Duty Cycle	V _{FB} =0.8V		92		%
Minimum On-Time			90		nS
Minimum Off-Time			60		nS
EN Input Current	V _{EN} =2V			1	uA
	V _{EN} =0V			1	uA
FB Input Current				1	uA
Under-Voltage Lockout Threshold-Hysteresis	On Threshold		3.4		V
	Off Threshold		3.1		V
Shutdown Threshold	Device ON		1.1		V
	Device OFF		1.0		V
EN up Threshold	V _{EN} -Rising	1.05	1.15	1.25	V
EN Threshold Hysteresis			140		mV
Soft Start			1		mS
Thermal Shutdown			150		°C
Thermal Hysteresis			20		°C

Note (1): MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.

Note (2): Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.

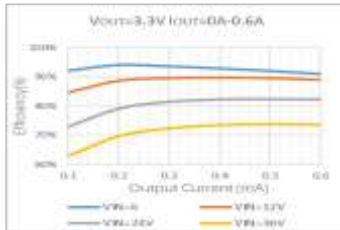
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Typical Performance Characteristics (1) (2)

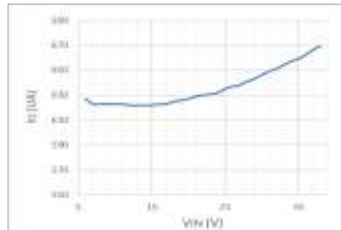
Note (1): Performance waveforms are tested on the evaluation board.

Note (2): $V_{IN}=12V$, $V_{OUT}=3.3V$, $T_A = +25^\circ C$, unless otherwise noted.

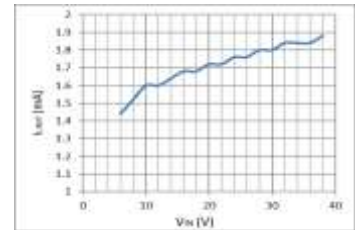
Efficiency Vs I_{OUT}



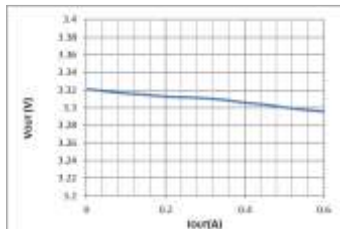
I_Q Vs V_{IN}



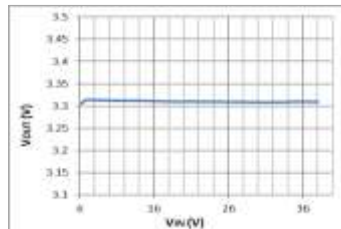
I_{LIMIT} Vs V_{IN}



V_{OUT} Vs I_{OUT}

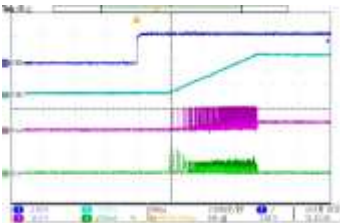


V_{OUT} VS V_{IN}



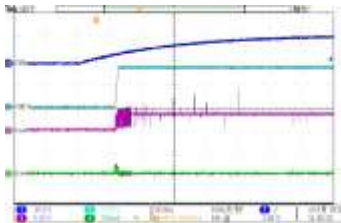
Start-up Waveform with EN

$V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{OUT}=0A$



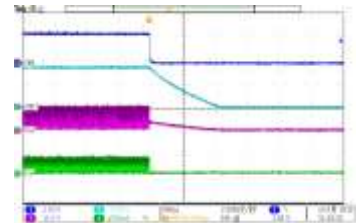
Start-up Waveform with EN= V_{IN}

$V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{OUT}=0A$



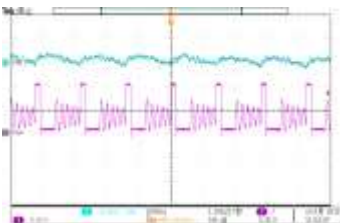
Shut-down Waveform with EN

$V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{OUT}=0.1A$



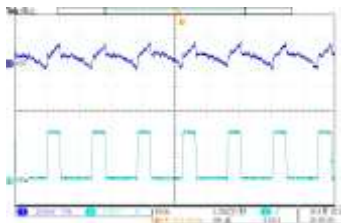
Switching Waveform

$V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{OUT}=0.06A$



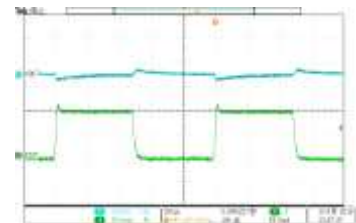
Switching Waveform

$V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{OUT}=0.6A$



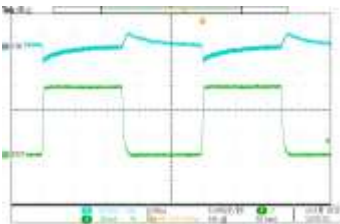
Load Transient Response

$V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{OUT}=0$ to $0.1A$



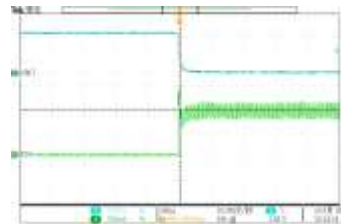
Load Transient Response

$V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{OUT}=0.01$ to $0.3A$



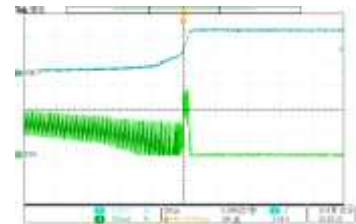
Short-Circuit Recovery

$V_{IN}=24V$, $V_{OUT}=3.3V$, $I_{OUT}=0A$ to Short



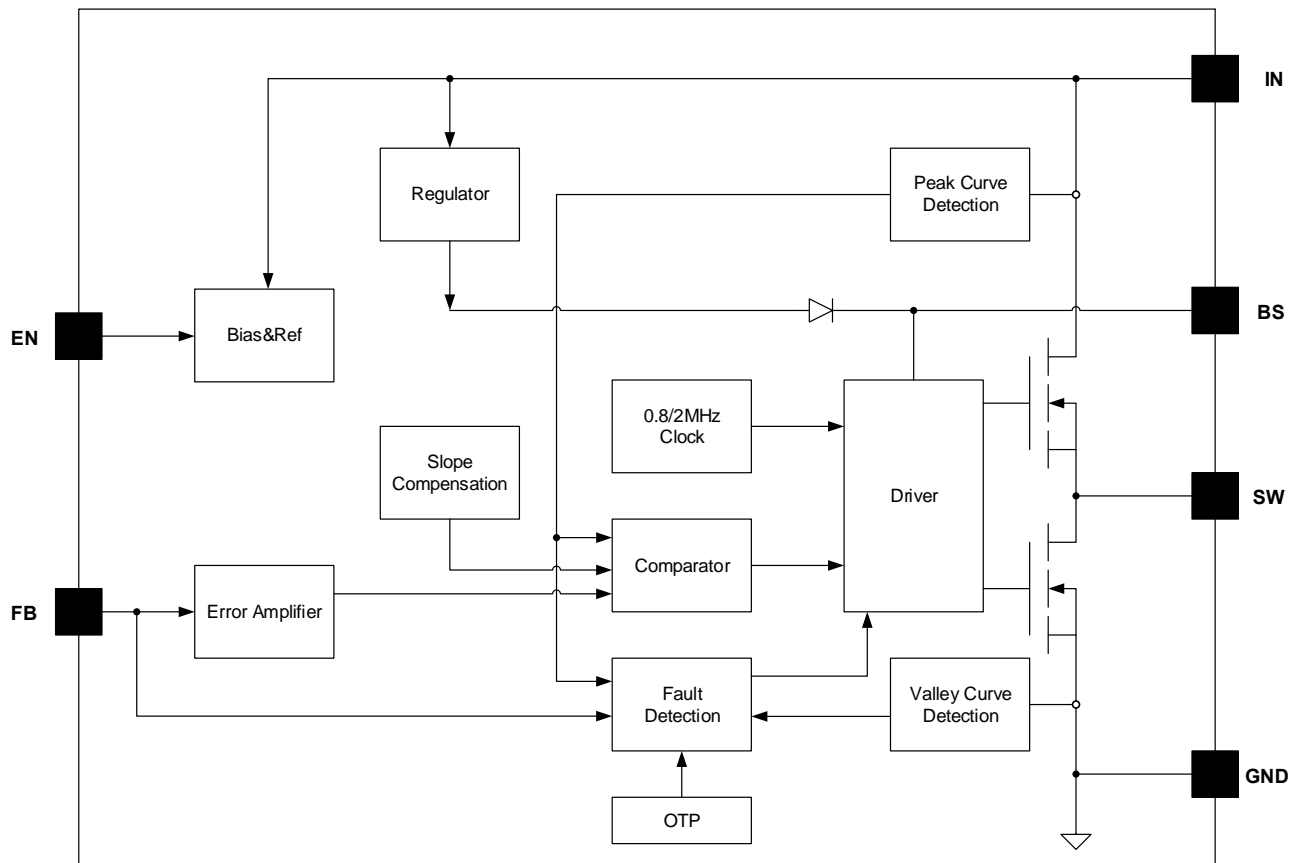
Short-Circuit Recovery

$V_{IN}=24V$, $V_{OUT}=3.3V$, $I_{OUT}=$ Short to $0A$



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Functional Block Diagram



J O : 338 Block Diagram

Functions Description

Internal Regulator

The J O : 338 is a current mode step down DC/DC converter that provides excellent transient response with no extra external compensation components. This device contains an internal, low resistance, high voltage power MOSFET, and operates at a high 800KHz operating frequency to ensure a compact, high efficiency design with excellent AC and DC performance.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal FB reference (VFB) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Internal Soft-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 0.8V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control. The SS time is internally max to 1ms.

Standoff 42V 0.6A 800kHz Sync Step-Down Regulator Over Current Protection & Hiccup

The J O : 338 has cycle-by-cycle over current limit when the inductor current peak value exceeds the set current limit threshold. Meanwhile, output voltage starts to drop until FB is below the Under-Voltage (UV) threshold, typically 25% below the reference. Once a UV is triggered, the J O : 338 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-short to ground. The average short circuit current is greatly reduced to alleviate the thermal issue and to protect the regulator. The J O : 338 exits the hiccup mode once the over current condition is removed.

Startup and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The comp voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

Applications Information

Setting the Output Voltage

J O : 338 require an input capacitor, an output capacitor and an inductor. These components are critical to the performance of the device. J O : 338 are internally compensated and do not require external components to achieve stable operation. The output voltage can be programmed by resistor divider.

$$V_{OUT} = V_{FB} \times \frac{R1 + R2}{R2}$$

V _{OUT} (V)	R1(KΩ)	R2(KΩ)	L1(μH)	C1(μF)	C _{FF} (pF)	C _{IN} (μF)	C _{OUT} (μF)
1	12.5	50	2.2	0.1	100~220	22	22~68
1.05	15.6	50	2.2	0.1	100~220	22	22~68
1.2	25	50	2.2	0.1	100~220	22	22~68
1.5	43.75	50	2.2	0.1	100~220	22	22~68
1.8	62.5	50	2.2	0.1	100~220	22	22~68
2.5	106.25	50	3.3	0.1	100~220	22	22~68
3.3	156.25	50	3.3	0.1	100~220	22	22~68
5.0	262.5	50	4.7	0.1	100~220	22	22~68

Resistor Selection for Common Output Voltages, C_{OUT}=22-68μF

Selecting the Inductor

The recommended inductor values are shown in the Application Diagram. It is important to guarantee the inductor core does not saturate during any foreseeable operational situation. The inductor should be rated to handle the peak load current plus the ripple current: Care should be taken when reviewing the different saturation current ratings that are specified by different manufacturers. Saturation current ratings are typically specified at 25 °C, so ratings at maximum ambient temperature of the application should be requested from the manufacturer.

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$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times F_{OSC}}$$

Where ΔI_L is the inductor ripple current. Choose inductor ripple current to be approximately 30% if the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

Selecting the Output Capacitor

Special attention should be paid when selecting these components. The DC bias of these capacitors can result in a capacitance value that falls below the minimum value given in the recommended capacitor specifications table.

The ceramic capacitor's actual capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of -55°C to $+125^{\circ}\text{C}$, will only vary the capacitance to within $\pm 15\%$. The capacitor type X5R has a similar tolerance over a reduced temperature range of -55°C to $+85^{\circ}\text{C}$. Many large value ceramic capacitors, larger than 1uF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C . Therefore X5R or X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C .

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47uF to 44uF range. Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to -40°C , so some guard band must be allowed.

PC Board Layout Consideration

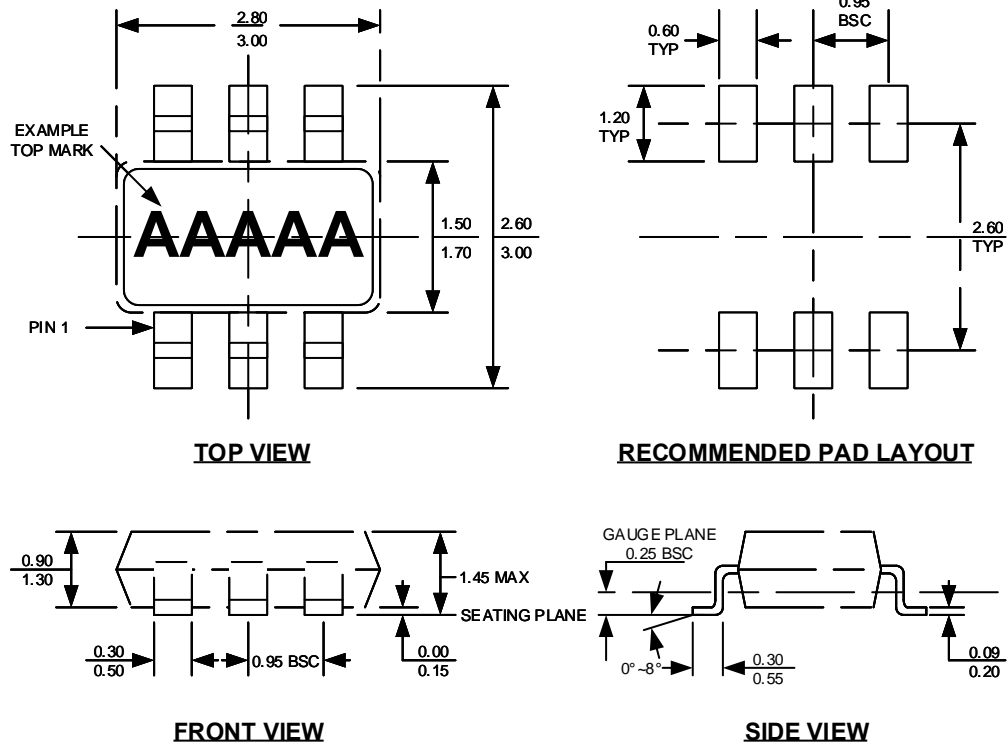
PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines for reference.

1. Keep the path of switching current short and minimize the loop area formed by Input capacitor, high-side MOSFET and low-side MOSFET.
2. Bypass ceramic capacitors are suggested to be put close to the Vin Pin.
3. Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4. VOUT, SW away from sensitive analog areas such as FB.
 Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

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Package Description

SOT23-6



NOTE:

1. CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5. DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6. DRAWING IS NOT TO SCALE.