

N-Channel Enhancement Mode Power MOSFET

Description

The HM100N07F uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.

General Features

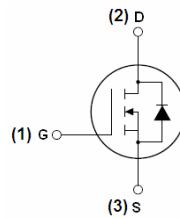
- $V_{DS} = 70V, I_D = 100A$
- $R_{DS(ON)} < 5.5 \text{ m}\Omega @ V_{GS}=10V$ (Typ:4.8mΩ)
- High density cell design for ultra low $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Special designed for converters and power controls
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard switched and High frequency circuits
- Uninterruptible power supply

100% UIS TESTED!

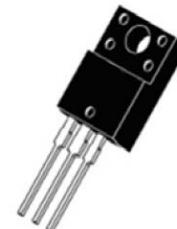
100% ΔVds TESTED!



Schematic diagram



Marking and pin assignment



TO-220F top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM100N07F	HM100N07F	TO-220F	-	-	-

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	70	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	100	A
Drain Current-Continuous($T_c=100^\circ\text{C}$)	$I_D(100^\circ\text{C})$	70.7	A
Pulsed Drain Current	I_{DM}	320	A
Maximum Power Dissipation	P_D	45	W
Derating factor		0.3	W/°C
Single pulse avalanche energy ^(Note 5)	E_{AS}	812	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	3.3	°C/W
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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

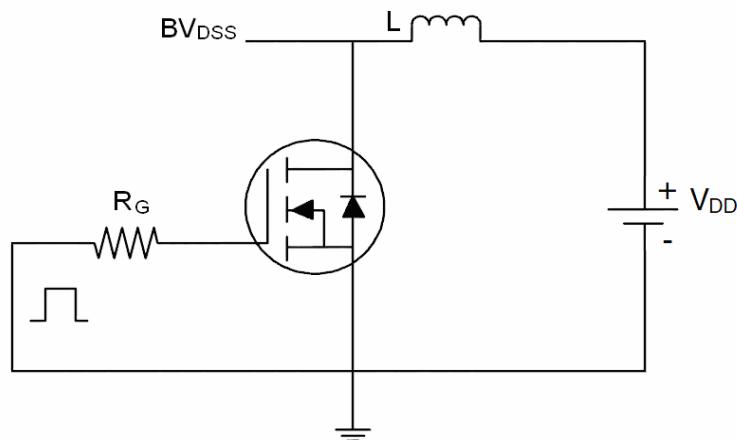
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_D=250\mu\text{A}$	70	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$\text{V}_{\text{DS}}=70\text{V}, \text{V}_{\text{GS}}=0\text{V}$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$\text{V}_{\text{GS}}=\pm 20\text{V}, \text{V}_{\text{DS}}=0\text{V}$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$\text{V}_{\text{GS(th)}}$	$\text{V}_{\text{DS}}=\text{V}_{\text{GS}}, \text{I}_D=250\mu\text{A}$	2	2.85	4	V
Drain-Source On-State Resistance	$\text{R}_{\text{DS(ON)}}$	$\text{V}_{\text{GS}}=10\text{V}, \text{I}_D=20\text{A}$	-	4.8	5.5	$\text{m}\Omega$
Forward Transconductance	g_{FS}	$\text{V}_{\text{DS}}=5\text{V}, \text{I}_D=20\text{A}$	-	50	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{iss}	$\text{V}_{\text{DS}}=25\text{V}, \text{V}_{\text{GS}}=0\text{V},$ $F=1.0\text{MHz}$	-	4900	-	PF
Output Capacitance	C_{oss}		-	380	-	PF
Reverse Transfer Capacitance	C_{rss}		-	290	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{\text{d(on)}}$	$\text{VDD}=35\text{V}, \text{RL}=15\Omega$ $\text{RG}=2.5\Omega, \text{VGS}=10\text{V}$	-	17	-	nS
Turn-on Rise Time	t_r		-	11	-	nS
Turn-Off Delay Time	$t_{\text{d(off)}}$		-	55	-	nS
Turn-Off Fall Time	t_f		-	15	-	nS
Total Gate Charge	Q_g	$\text{V}_{\text{DS}}=35\text{V}, \text{I}_D=20\text{A},$ $\text{V}_{\text{GS}}=10\text{V}$	-	100	-	nC
Gate-Source Charge	Q_{gs}		-	21	-	nC
Gate-Drain Charge	Q_{gd}		-	30	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_s=20\text{A}$	-	-	1.2	V
Diode Forward Current (Note 2)	I_s		-	-	100	A
Reverse Recovery Time	t_{rr}	$\text{Tj}=25^\circ\text{C}, \text{I}_F=100\text{A}$ $\text{di}/\text{dt}=100\text{A}/\mu\text{s}$ (Note 3)	-		37	nS
Reverse Recovery Charge	Q_{rr}		-		58	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

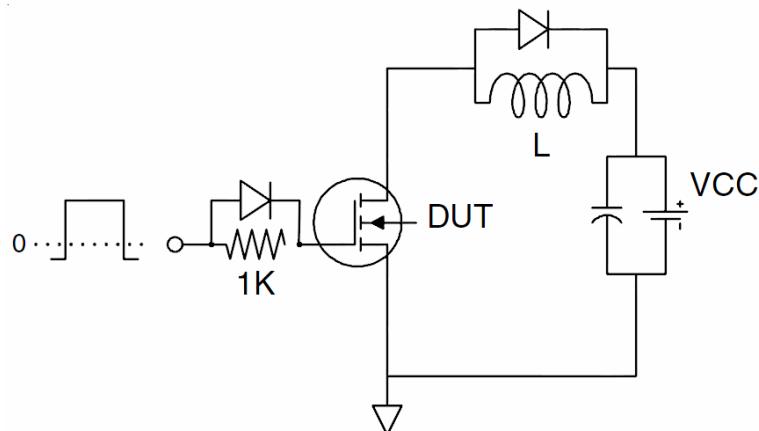
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $\text{Tj}=25^\circ\text{C}, \text{V}_{\text{DD}}=35\text{V}, \text{V}_{\text{G}}=10\text{V}, \text{L}=0.5\text{mH}, \text{Rg}=25\Omega$

Test Circuit

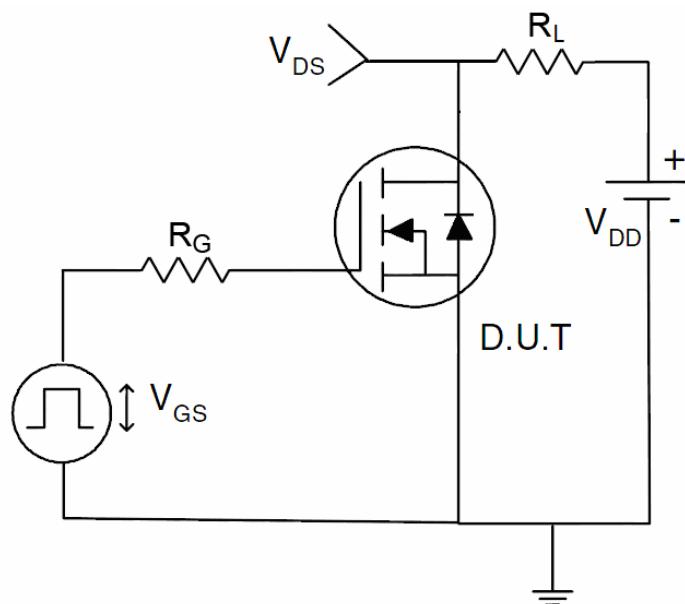
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

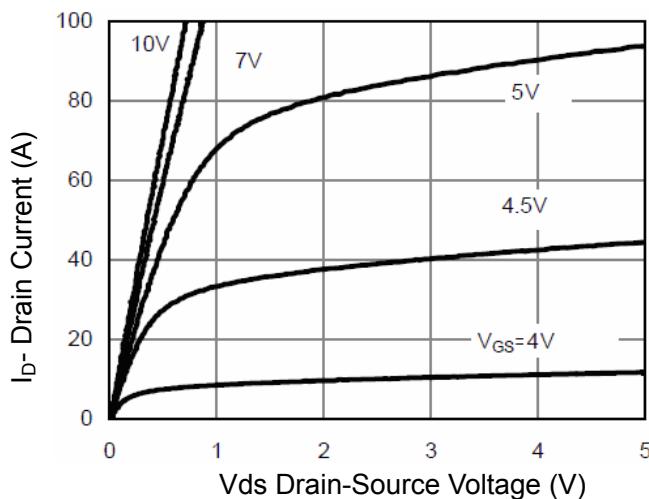


Figure 1 Output Characteristics

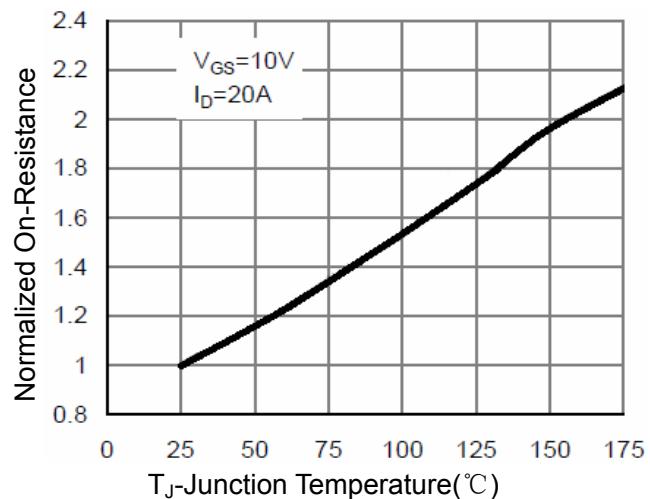


Figure 4 Rdson-Junction Temperature

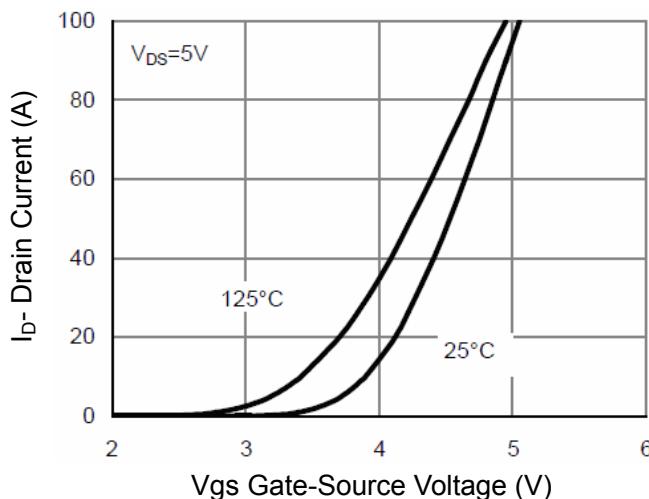


Figure 2 Transfer Characteristics

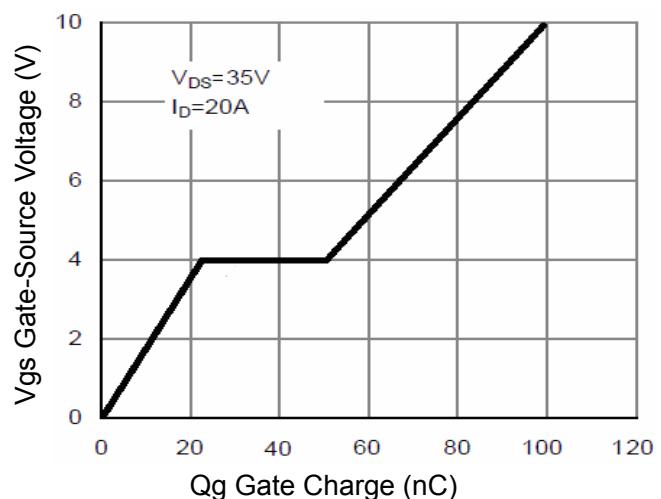


Figure 5 Gate Charge

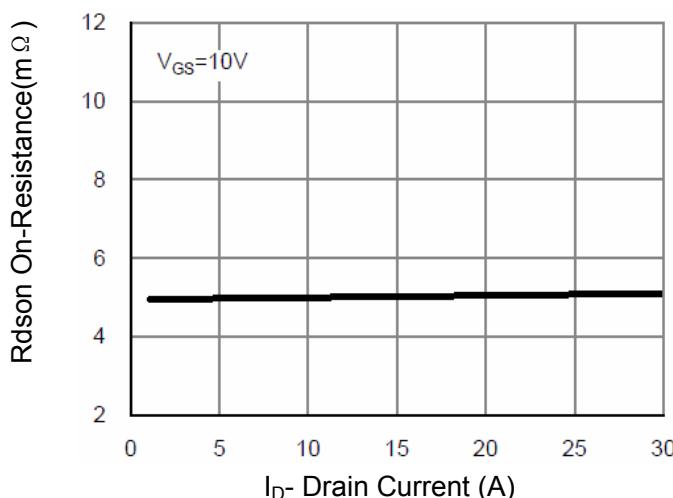


Figure 3 Rdson- Drain Current

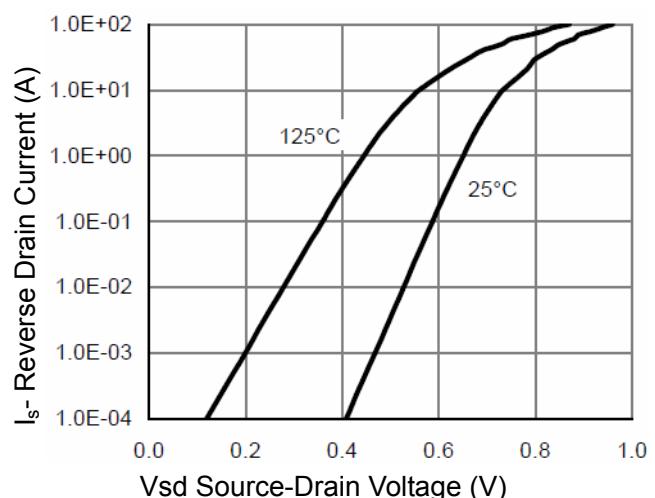


Figure 6 Source- Drain Diode Forward

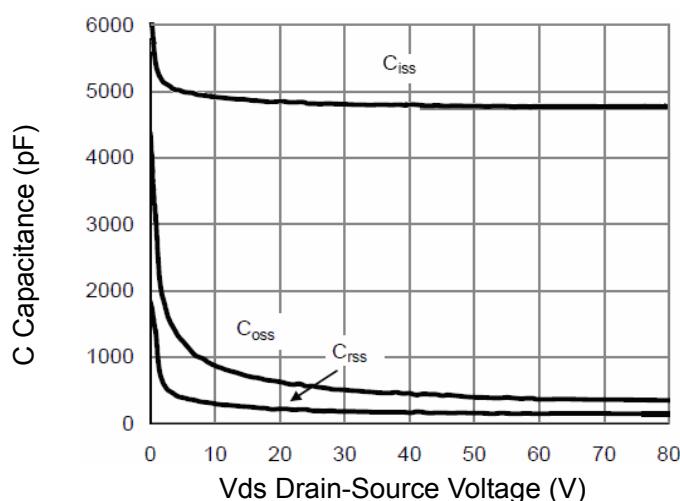


Figure 7 Capacitance vs Vds

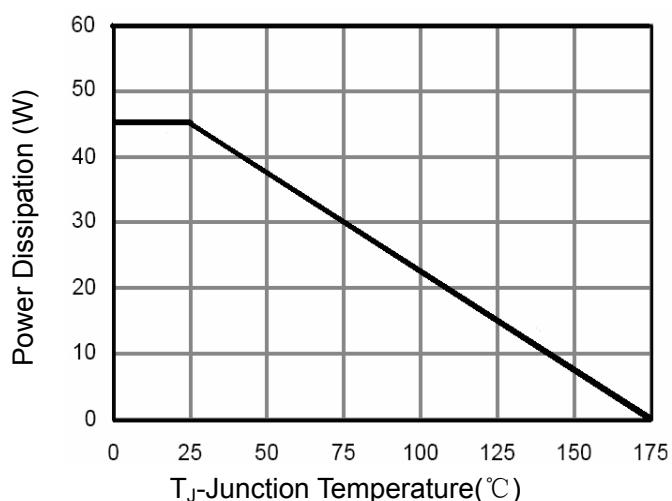


Figure 9 Power De-rating

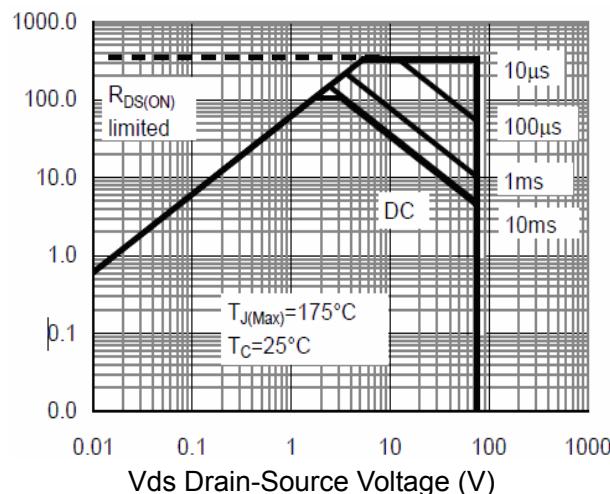


Figure 8 Safe Operation Area

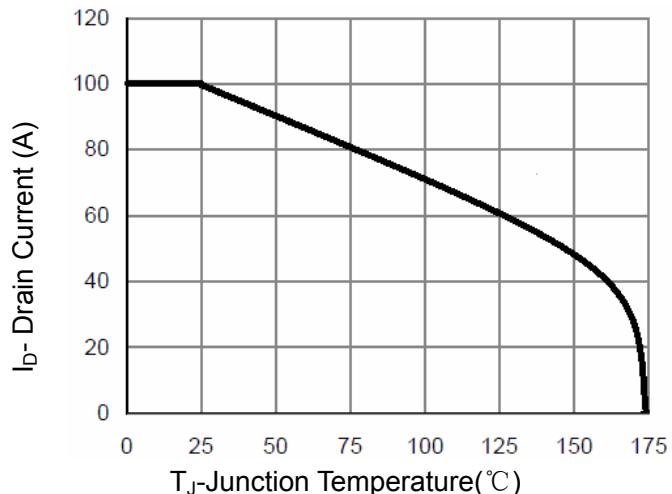


Figure 10 I_D Current De-rating

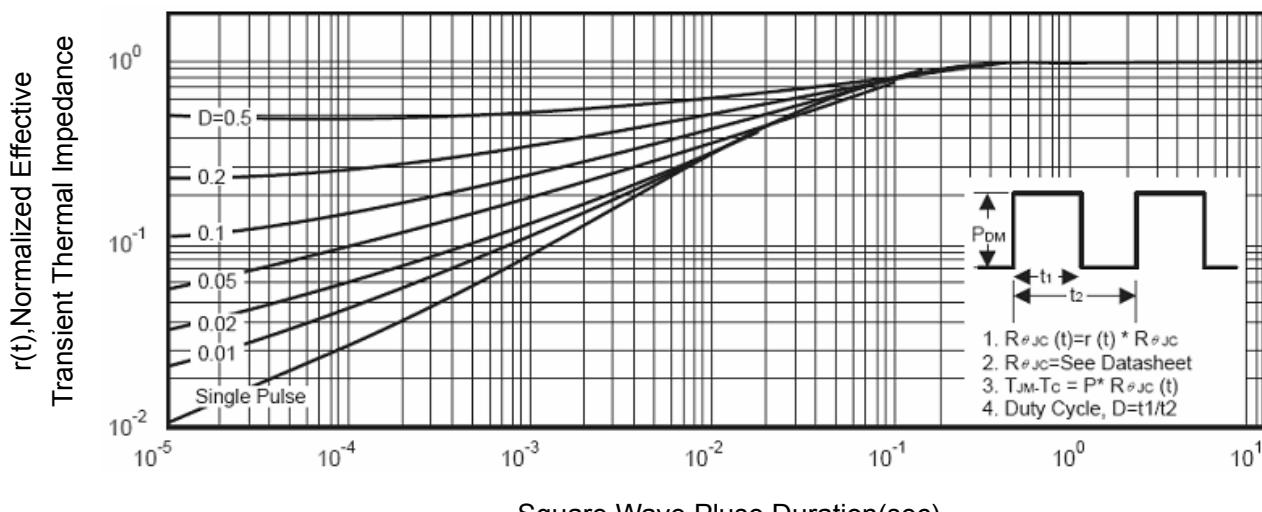
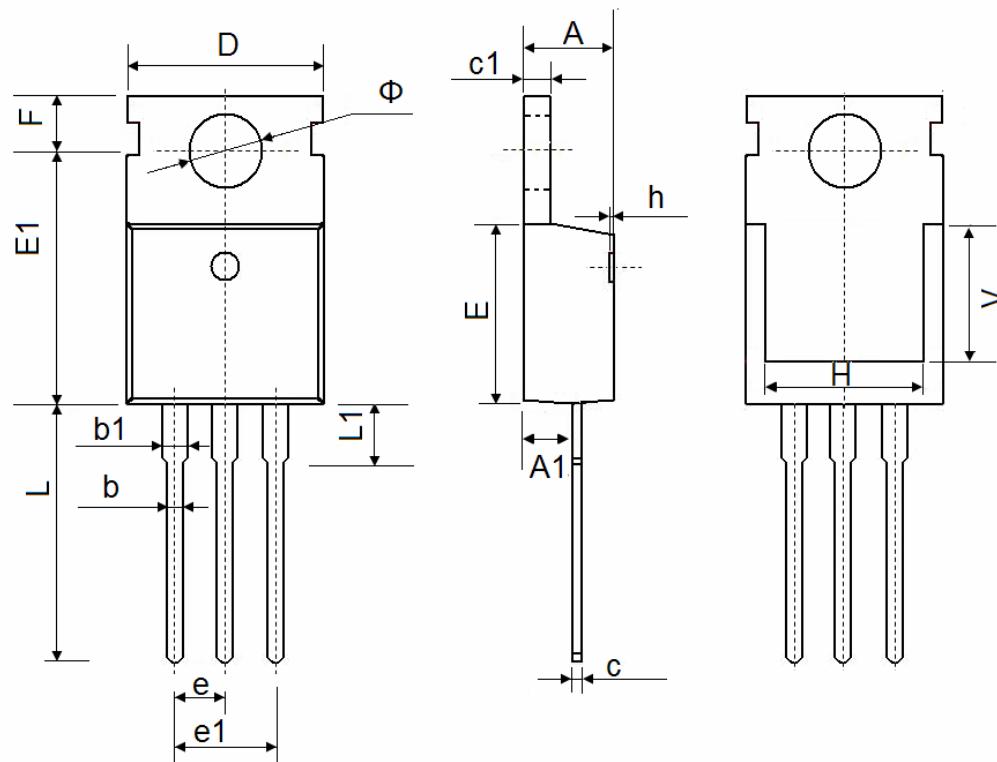


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-220-3L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.9500	9.750	0.352	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	7.500 REF.		0.295 REF.	
Φ	3.400	3.800	0.134	0.150