

0.3 μ A I_Q , High PSRR, 500mA Low-Dropout Linear Voltage

Features

- Low Quiescent Current: 0.3 μ A
- PSRR=70dB@1KHz
- Wide Operating Input Voltage Range:
2V to 7V
- High Output Current: ≥ 500 mA
- Dropout Voltage:
100mV@100mA (3.3V)
- $\pm 1.5\%$ Output Accuracy
- Good Transient Response
- Integrated Short-Circuit Protection
- Over-Temperature Protection
- Support Fixed Output Voltage
0.9V/1.0V/1.2V/1.5V/1.8
2.5V/2.8V/3.0V/3.3V/3.6V
- Available Package:
SOT23-5L, SOT23-3L, SOT89-3L

Applications

- Portable, Battery Powered Equipment
- Ultra Low Power Microcontrollers
- Notebook Computers
- Audio/Video Equipment
- Weighting Scales
- Home Automation

General Description

The HM6234 is a low-dropout (LDO) voltage regulator with enable function that operates from a 2.0V to 7V supply. It provides up to 500mA of output current in miniaturized packaging.

The features of low quiescent current as low as 0.3 μ A and almost zero disable current is ideal for powering battery equipment to a longer service life. The other features include current limit function, over temperature protection and output discharge function.

Application Circuits

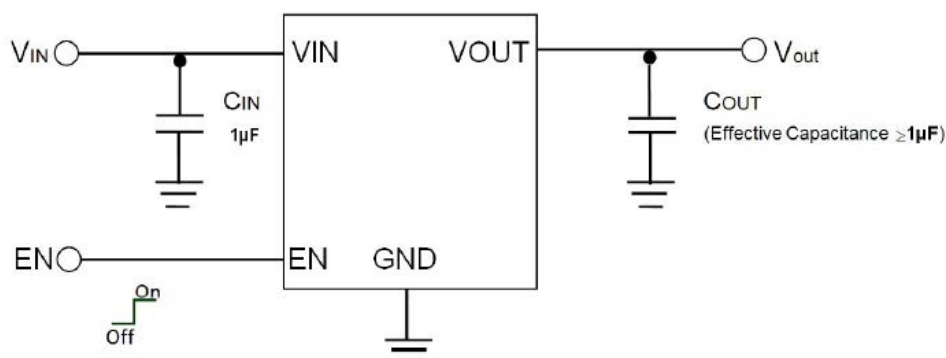
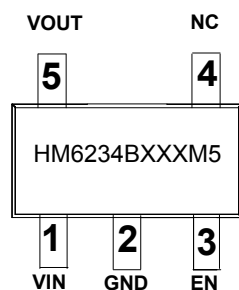
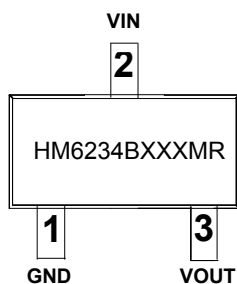


Figure 1. Typical Application Circuit

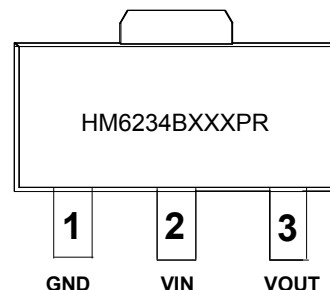
Pin Configuration



SOT23-5L



SOT23-3L



SOT89-3L

Pin Description

Pin No.			Pin Name	Pin Function
SOT23-5L	SOT23-3L	SOT89-3L		
1	2	2	VIN	Supply voltage input.
2	1	1	GND	Ground.
3	----	----	EN	Enable control input.
4	----	----	NC	No Internal Connection.
5	3	3	VOUT	Output of the regulator.

Order Information

HM6234B ③④ ①②

Designator	Symbol	Description
①②	M5\MP	SOT23-5L\ SOT23-3L\ SOT89-3L
③④	Integer	Output Voltage(09、10、12、15、18、25、28、30、33、36)
⑤	R	RoHS / Pb Free
	G	Halogen Free

Marking Information:

34XX: 34: 产品型号 XX: 输出电压

Absolute Maximum Ratings ^{(1) (2)}

Item	Description	Min	Max	Unit
Voltage	V_{IN} , V_{EN} to GND	-0.3	9	V
	V_{OUT} to GND	-0.3	9	V
	V_{OUT} to V_{IN}	-0.3	$V_{IN}+0.3$	V
Power dissipation	SOT23-5L	0.45		W
	SOT23-3L	0.45		W
	SOT89-3L	0.50		W
Thermal Resistance	SOT23-5L; θ_{JA}	220		°C /W
	SOT23-3L; θ_{JA}	220		°C /W
	SOT89-3L; θ_{JA}	200		°C /W
Operating Ambient Temperature		-25	85	°C
Maximum junction temperature		-40	125	°C
Storage temperature, T_{stg}		-55	155	°C

Note (1): Exceeding these ratings may damage the device.

Note (2): The device is not guaranteed to function outside of its operating conditions.

ESD Ratings

Item	Description	Value	Unit
$V(ESD-HBM)$	Human Body Model (HBM) ANSI/ESDA/JEDEC JS-001-2014 Classification, Class: 2	±4000	V
$V(ESD-CDM)$	Charged Device Mode (CDM) ANSI/ESDA/JEDEC JS-002-2014 Classification, Class: C0b	±200	V
ILATCH-UP	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	±150	mA

Recommended Operating Conditions

Item	Min	Max	Unit
Operating junction temperature ⁽¹⁾	-25	85	°C
Input voltage V_{IN}	2	7	V

Note (1): All limits specified at room temperature ($T_A = 25^{\circ}\text{C}$) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Electrical Characteristics

(At $T_A=25^{\circ}\text{C}$, $C_{IN}=1\mu\text{F}$, $V_{IN}=V_{OUT}+1.0\text{V}$, $V_{OUT}=3.3\text{V}$, $C_{OUT}=1\mu\text{F}$, unless otherwise noted)

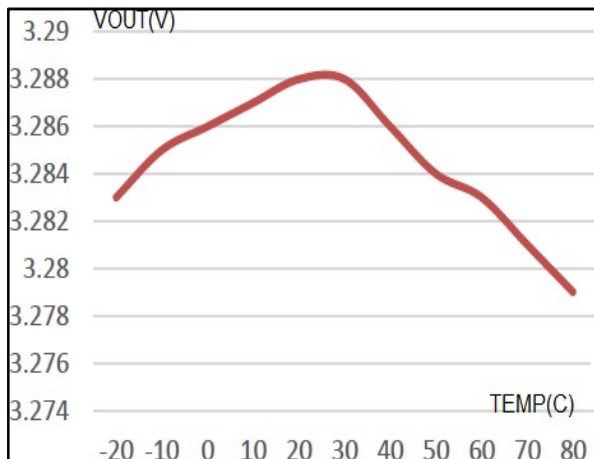
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Units
V_{IN}	Input Voltage		2	—	7	V
I_Q	Quiescent Current	$V_{IN} > V_{OUT}$, $EN=V_{IN}$ No load	—	0.3	0.7	μA
V_{OUT}	Output Voltage	$I_{OUT}=1\text{mA}$	-1.5		+1.5	%
I_{SD}	Shutdown Ground Current	$V_{EN}=0\text{V}$	—	—	0.1	μA
I_{LEAK}	V_{OUT} Shutdown Leakage Current	$V_{OUT}=0\text{V}$	—	—	0.1	μA
I_{OUT_MAX}	Output Current	$V_{IN}-V_{OUT}=0.5\text{V}$	—	500	—	mA
V_{DROP}	Dropout Voltage(1)	$I_{OUT}=100\text{mA}$ $V_{OUT}=3.3\text{V}$	—	100	120	mV
		$I_{OUT}=200\text{mA}$ $V_{OUT}=3.3\text{V}$	—	200	250	mV
ΔLOAD	Load Regulation	$V_{IN}=V_{OUT}+1\text{V}$ $1\text{mA}\leq I_{OUT}\leq 300\text{mA}$	—	20	30	mV
ΔLINE	Line Regulation	$I_{OUT}=1\text{mA}$, $V_{OUTNOM}+0.5\text{V}\leq V_{IN}\leq 7\text{V}$	—	0.1	0.15	%/V
I_{LIMIT}	Current Limit	$V_{IN}=5\text{V}$	—	550	—	mA
PSRR	Power Supply Rejection Ratio	$I_{OUT}=100\text{mA}$ $f=10\text{KHz}$		65		dB
		$I_{OUT}=100\text{mA}$ $f=1\text{KHz}$		70		dB
I_{SHORT}	Short /Start Load Current	$R_L=1\Omega$		90		mA
V_{IH}	EN Threshold Voltage,Logic-High	$V_{IN}=5.0\text{V}$, $I_{OUT}=1\text{mA}$	1.2	—	—	V
V_{IL}	EN Threshold Voltage,Logic-Low	$V_{IN}=5.0\text{V}$	—	—	0.4	V
e_{NO}	Output Noise Voltage	10Hz to 100kHz $C_{OUT}=1\mu\text{F}$	—	100	—	μVRMS
T_{SD}	Thermal Shutdown Temperature		—	160	—	$^{\circ}\text{C}$
ΔT_{SD}	Thermal Shutdown Hysteresis		—	20	—	$^{\circ}\text{C}$

Note: (1) Dropout Voltage is the voltage difference between the input and the output at which the output voltage drops 2% below its nominal value.

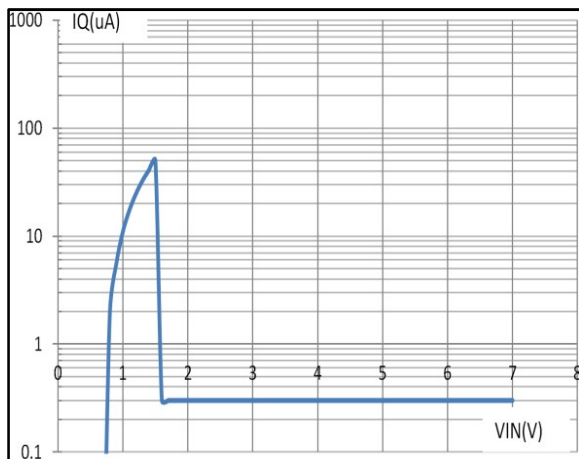
Typical Performance Characteristics

Test Condition: $T_A=25^{\circ}\text{C}$, unless otherwise note

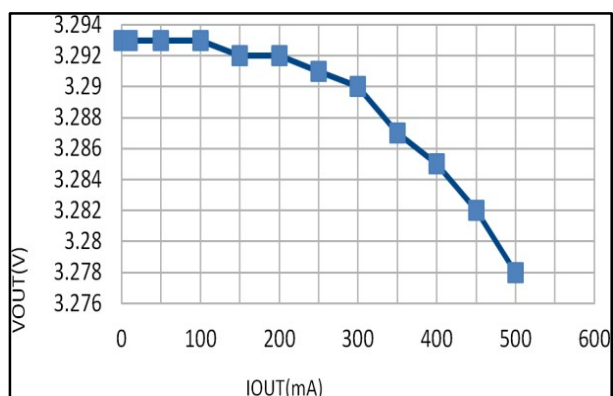
1、VOUT vs TEMP



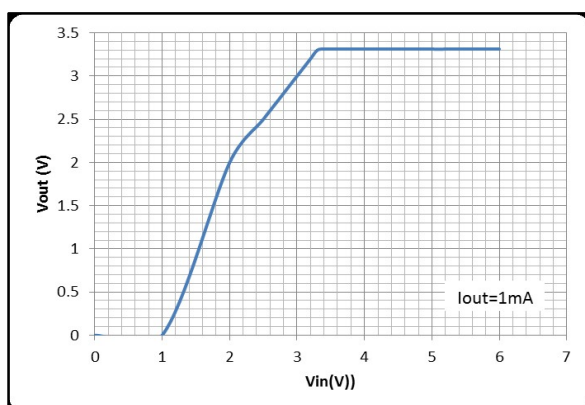
2、IQ vs VIN (※)



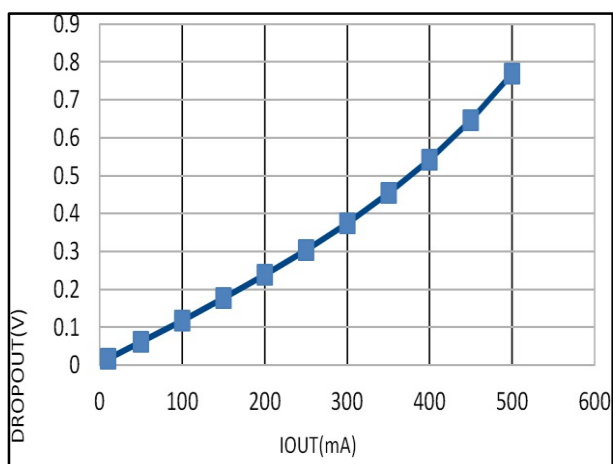
3、Load Regulation



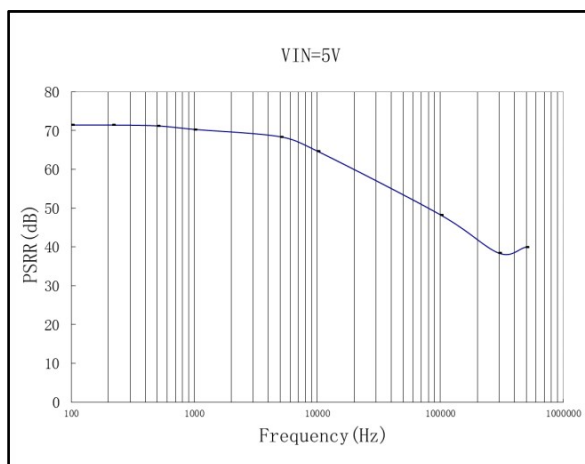
4、Line Regulation



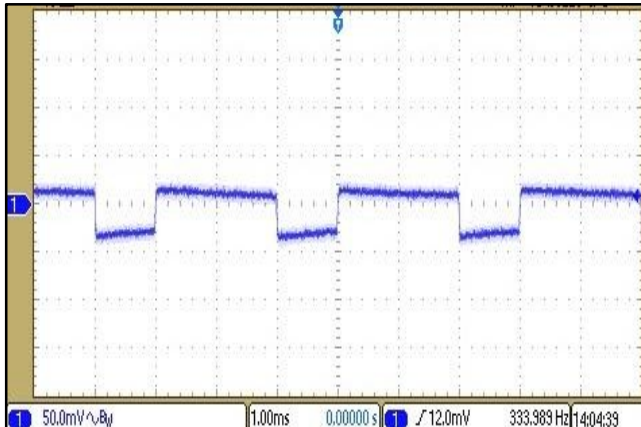
5、Dropout Voltage vs Load Current



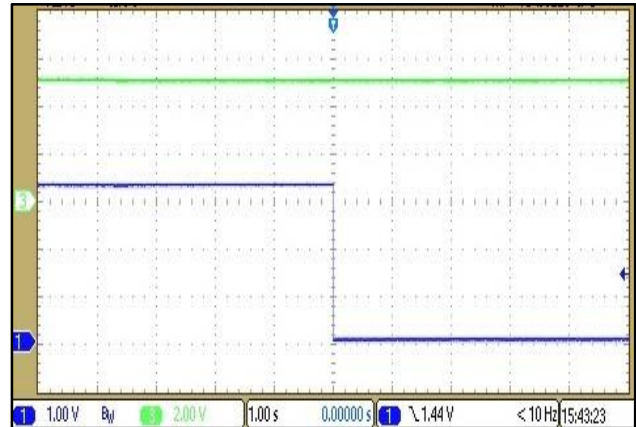
6、PSRR



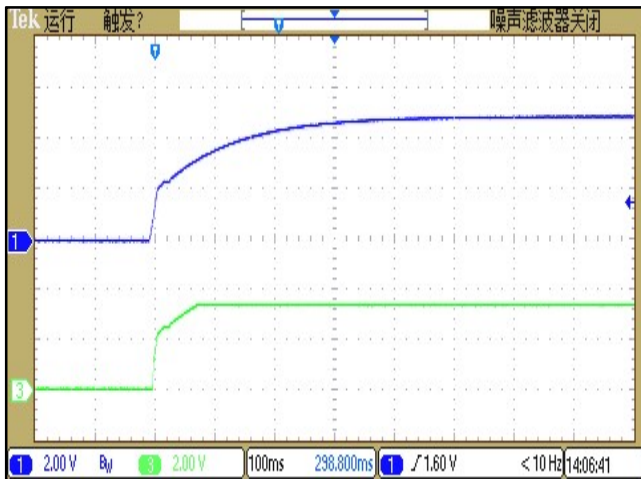
7、Load Transient Response



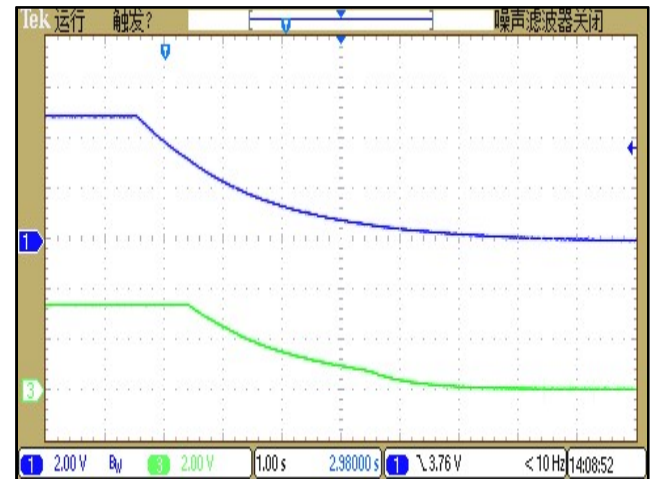
8、Short Output & Over-Current Response



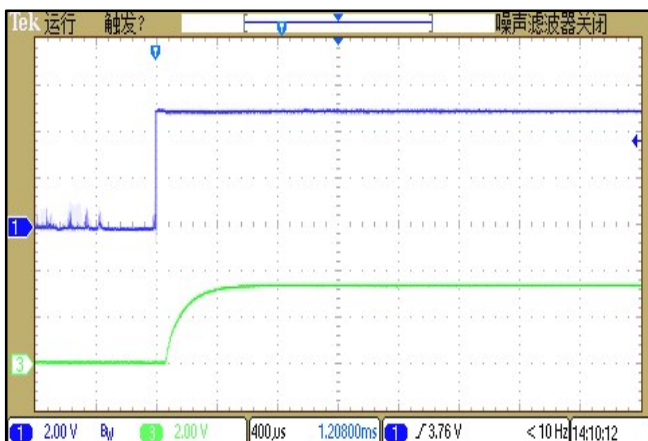
9、Power-On



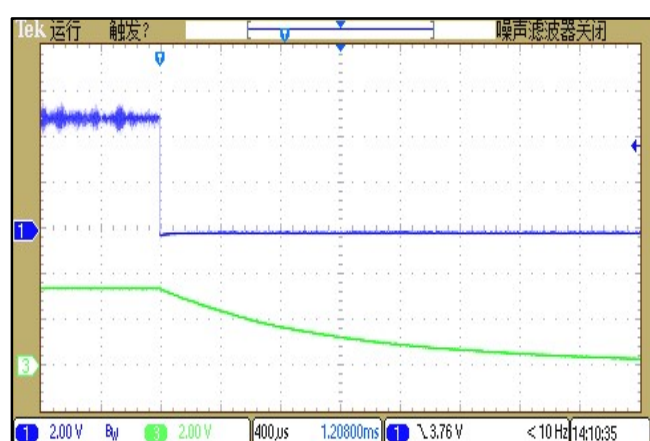
10、Power-Off



11、Enable

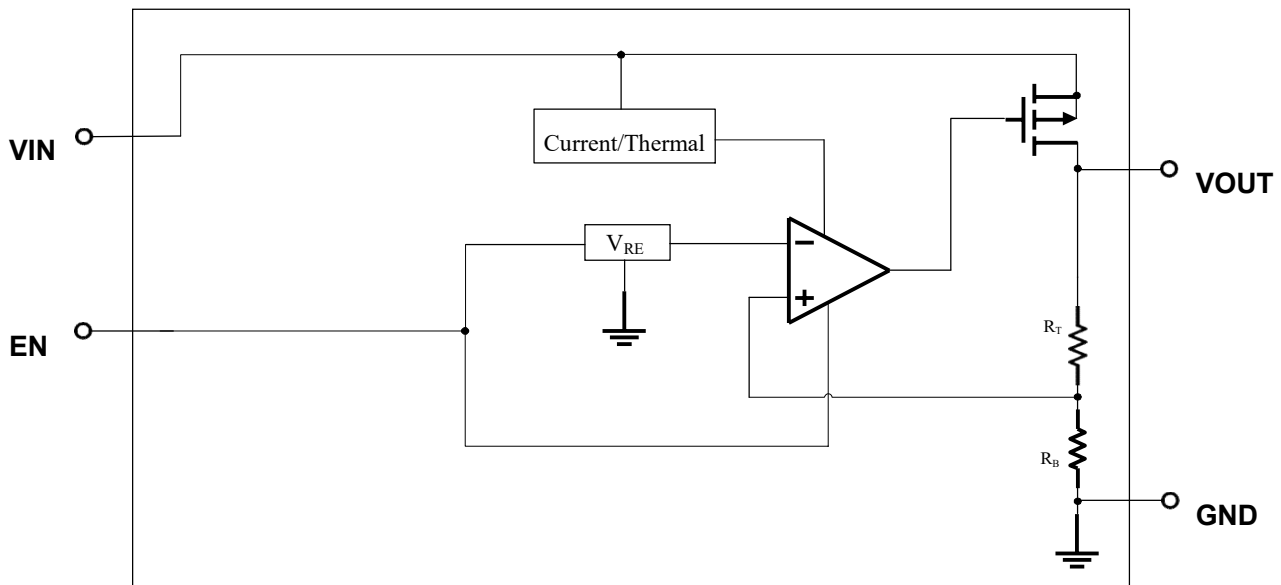


12、Disable



Note: (※)IQ refers to the working current when the chip is no-load, only when $V_{in} > V_{out}$ The chip will have a very low working current, the above diagram is for V_{out} 1.5v Measured Curve, when $V_{in} < V_{out}$, the chip is in an abnormal state that can not reach the intended output, therefore, the operating current will increase significantly. For applications where IQ requirements are strict, make sure the chip stops working when $V_{in} < V_{out}$.

Function Block Diagram



Application Guideline

Input Capacitor

A 1 μ F ceramic capacitor is recommended to connect between **V_{DD}** and **GND** pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both **VIN** and **GND**.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is 1 μ F, ceramic capacitor is recommended, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to **VOUT** and **GND** pins.

Dropout Voltage

The dropout voltage refers to the voltage difference between the **VIN** and **VOUT** pins while operating at specific output current. The dropout voltage **V_{DROP}** also can be expressed as the voltage drop on the pass-FET at specific output current (**I_{RATED}**) while the pass-FET is fully operating at ohmic region and the pass-FET can be characterized as a resistance **R_{DS(ON)}**. Thus the dropout voltage can be defined as

($V_{DRO} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{RATED}$). For normal operation, the suggested LDO operating range is ($V_{IN} > V_{OUT} + V_{DRO}$) for good transient response and PSRR ability. Vice versa, while operating at the ohmic region will degrade the performance severely.

Thermal Application

For continuous operation, do not exceed the absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated as below: $T_A=25^{\circ}\text{C}$, PCB,

The max PD(Max)= $(125^{\circ}\text{C} - 25^{\circ}\text{C}) / (220^{\circ}\text{C/W}) = 0.45\text{W}$ for SOT-23-5 packages.

The max PD(Max)= $(125^{\circ}\text{C} - 25^{\circ}\text{C}) / (220^{\circ}\text{C/W}) = 0.45\text{W}$ for SOT-23-3 packages.

The max PD(Max)= $(125^{\circ}\text{C} - 25^{\circ}\text{C}) / (200^{\circ}\text{C/W}) = 0.50\text{W}$ for SOT-89-3 packages.

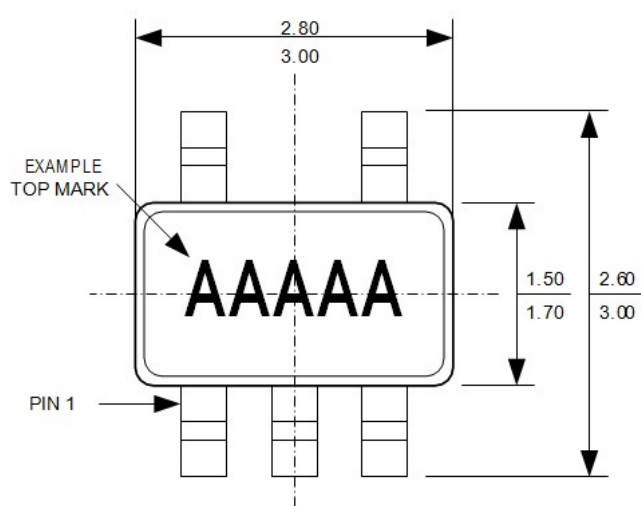
Power dissipation (PD) is equal to the product of the output current and the voltage drop across the output pass element, as shown in the equation below:

$$PD = (V_{IN} - V_{OUT}) \times I_{OUT}$$

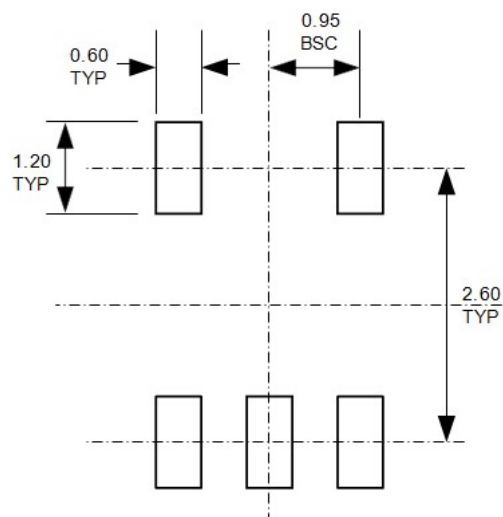
Layout Consideration

By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the HM6234 ground pin using as wide and as short of a copper trace as is practical. Connections using long trace lengths, narrow trace widths, and/or connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.

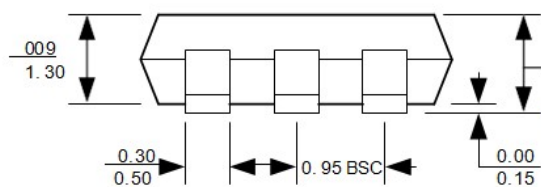
Packaging Information SOT23-5L



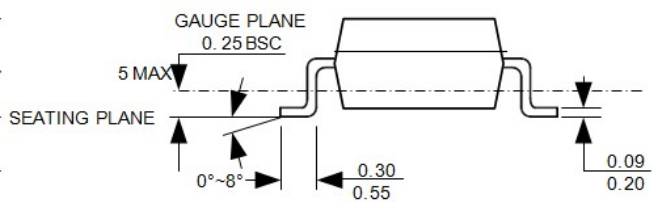
TOP VIEW



RECOMMENDED PAD LAYOUT

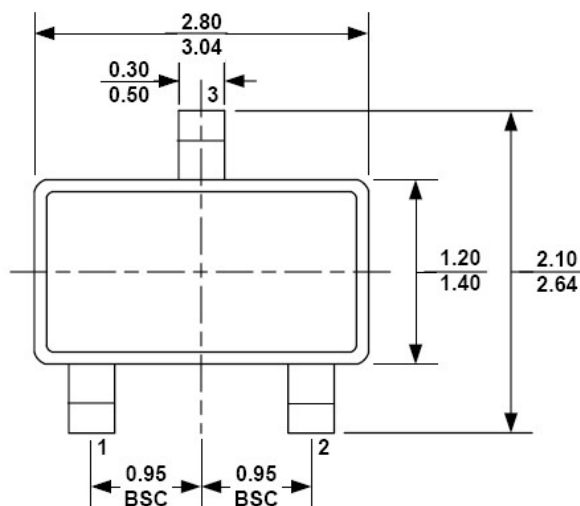


FRONT VIEW

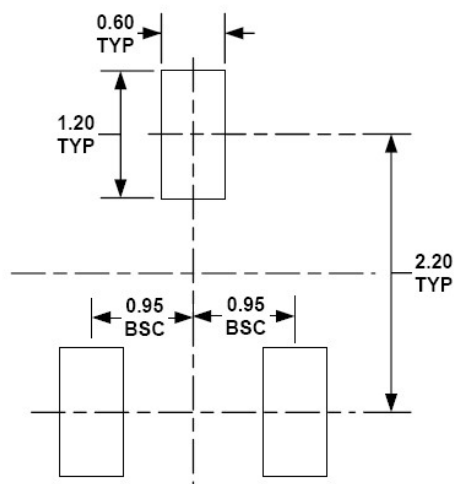


SIDE VIEW

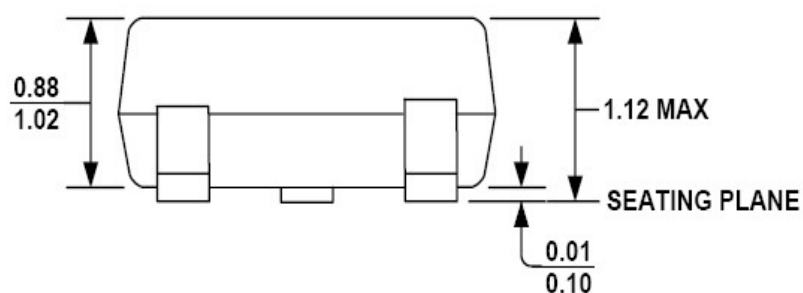
Packaging Information SOT23-3L



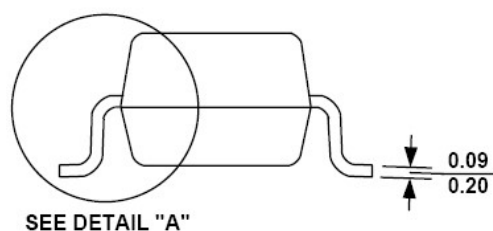
TOP VIEW



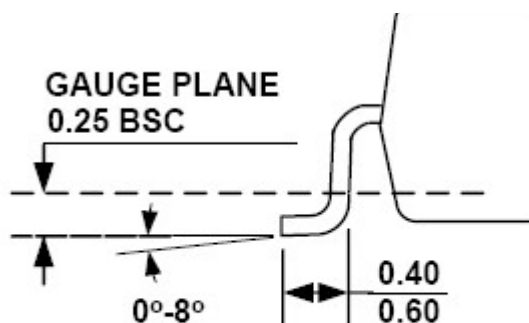
RECOMMENDED LAND PATTERN



FRONT VIEW

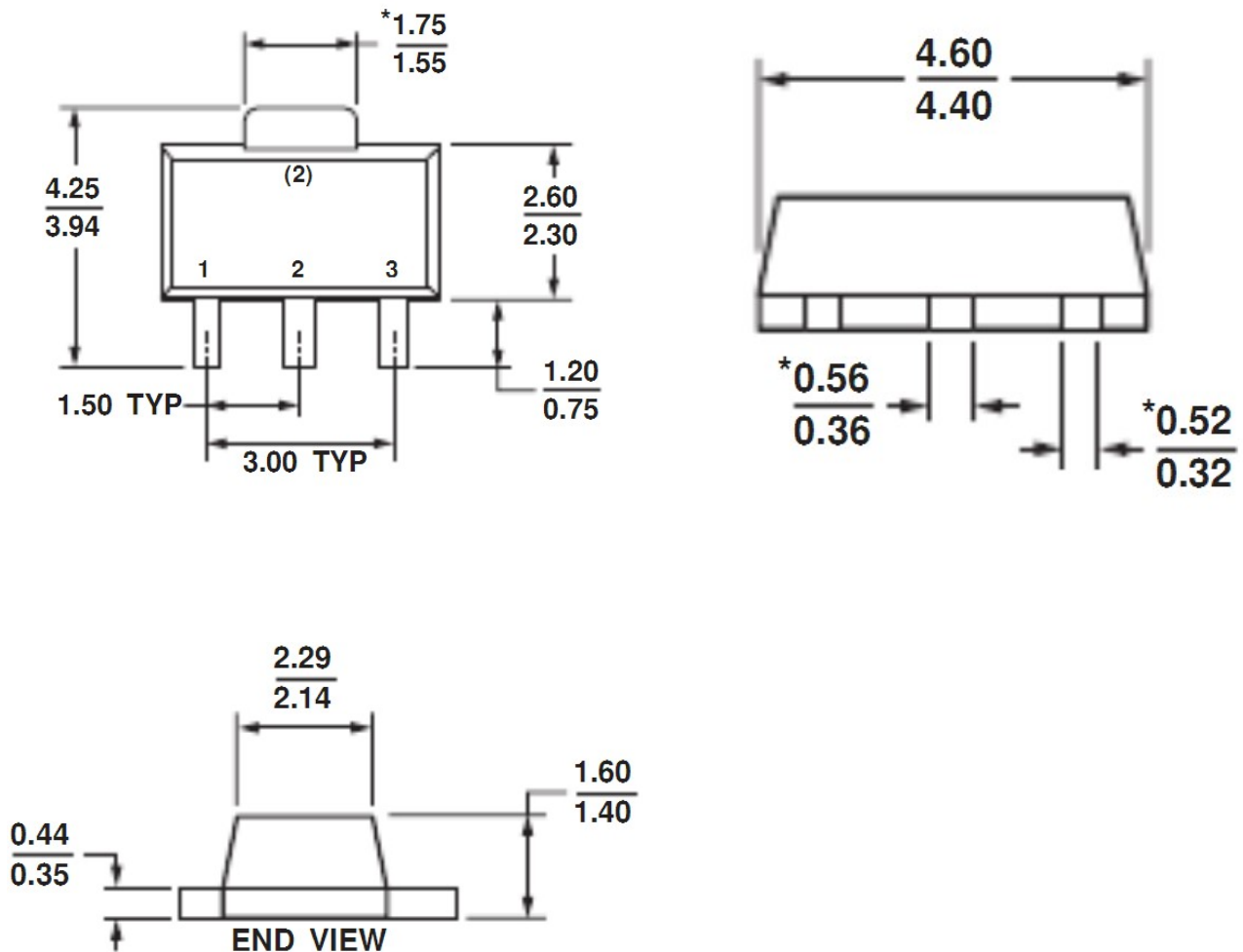


SIDE VIEW



DETAIL "A"

Packaging Information SOT89-3L



NOTE:

1. CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5. DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6. DRAWING IS NOT TO SCALE.