

## N-Channel Enhancement Mode Power MOSFET

### Description

The HMS18N10Q uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

### General Features

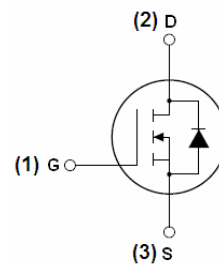
- $V_{DS} = 100V, I_D = 18A$   
 $R_{DS(ON)} < 6m\Omega @ V_{GS} = 10V$  (Typ: 75m $\Omega$ )  
 $R_{DS(ON)} < 8m\Omega @ V_{GS} = 4.5V$  (Typ: 80m $\Omega$ )
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

### Application

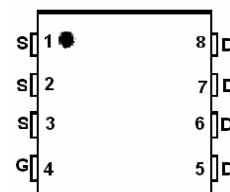
- Power switching application
- Hard switched and high frequency circuits

**100% UIS TESTED!**

**100%  $\Delta V_{ds}$  TESTED!**



Schematic diagram



Marking and pin assignment

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HMS18N10Q	HMS18N10Q	DFN3X3-8L			

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	18	A
Drain Current-Continuous ( $T_C = 100^\circ C$ )	$I_D (100^\circ C)$	13	A
Pulsed Drain Current	$I_{DM}$	54	A
Maximum Power Dissipation	$P_D$	50	W
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	16	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ C$

## Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	3	$^{\circ}C/W$
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## Electrical Characteristics ( $T_C=25^{\circ}C$ unless otherwise noted)

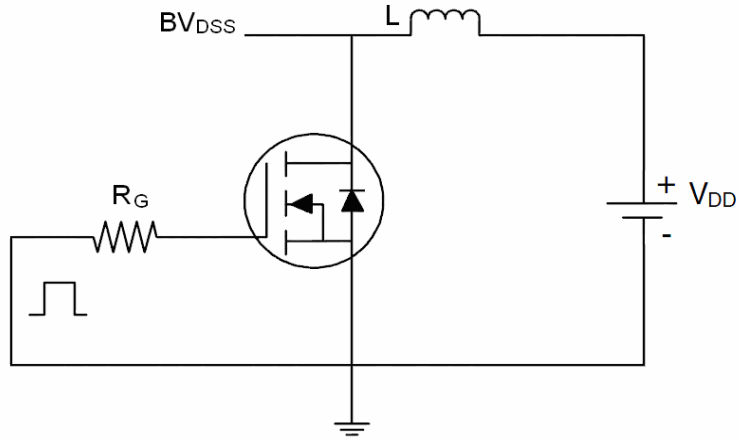
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	100	110	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=100V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> <sup>(Note 3)</sup>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.1	-	2.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=18A$	-	-	23	m $\Omega$
		$V_{GS}=4.5V, I_D=18A$	-	-	33	
Forward Transconductance	$g_{FS}$	$V_{DS}=5V, I_D=18A$	-	10	-	S
<b>Dynamic Characteristics</b> <sup>(Note 4)</sup>						
Input Capacitance	$C_{iss}$	$V_{DS}=50V, V_{GS}=0V,$ $F=1.0MHz$	-	830	-	PF
Output Capacitance	$C_{oss}$		-	44.2	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	30.1	-	PF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=50V, R_L=6.4\Omega$ $V_{GS}=10V, R_G=3\Omega$	-	15	-	nS
Turn-on Rise Time	$t_r$		-	5	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	25	-	nS
Turn-Off Fall Time	$t_f$		-	7	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=50V, I_D=18A,$ $V_{GS}=10V$	-	22.3	-	nC
Gate-Source Charge	$Q_{gs}$		-	2.87	-	nC
Gate-Drain Charge	$Q_{gd}$		-	6.14	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note 3)</sup>	$V_{SD}$	$V_{GS}=0V, I_S=18A$	-	-	1.2	V
Diode Forward Current <sup>(Note 2)</sup>	$I_S$		-	-	18	A

## Notes:

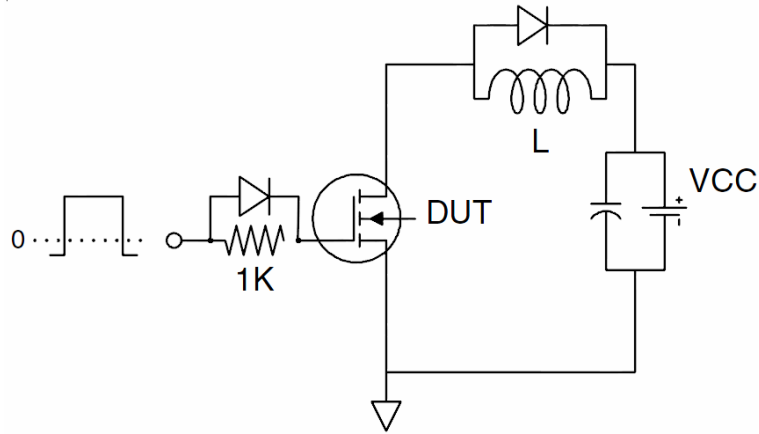
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition:  $T_j=25^{\circ}C, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

## Test Circuit

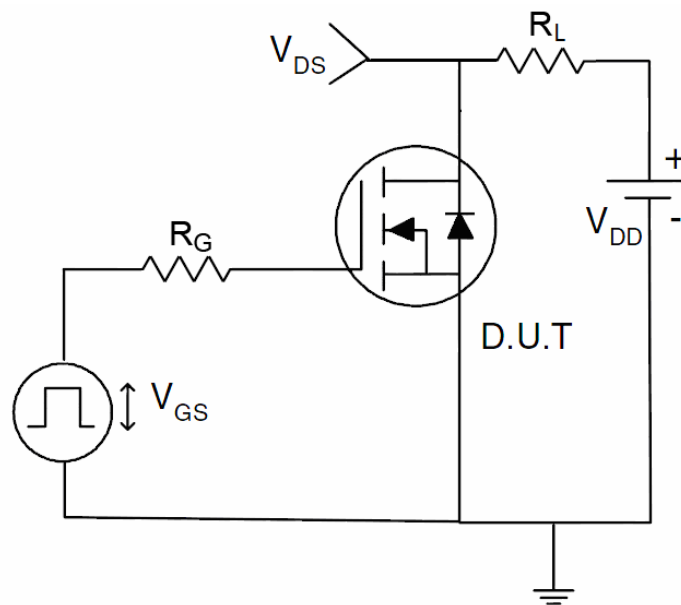
### 1) E<sub>AS</sub> test Circuit



### 2) Gate charge test Circuit



### 3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

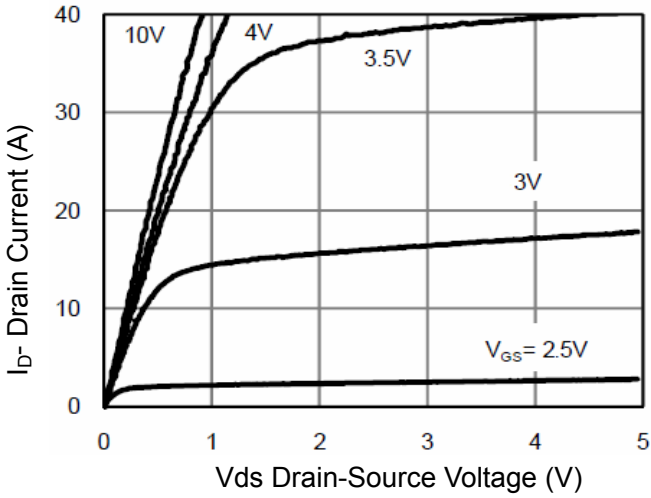


Figure 1 Output Characteristics

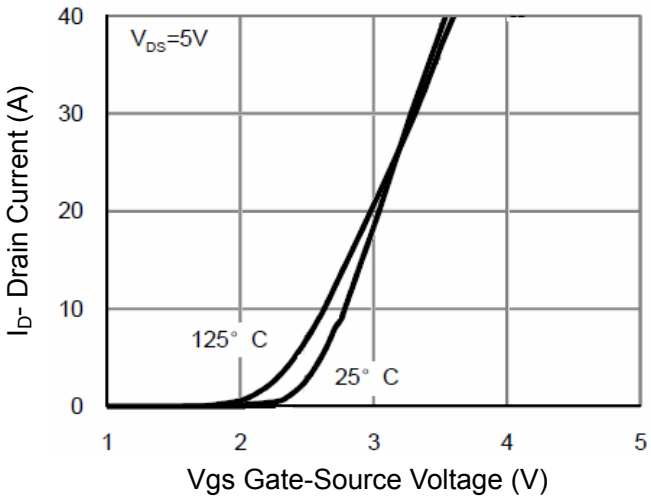


Figure 2 Transfer Characteristics

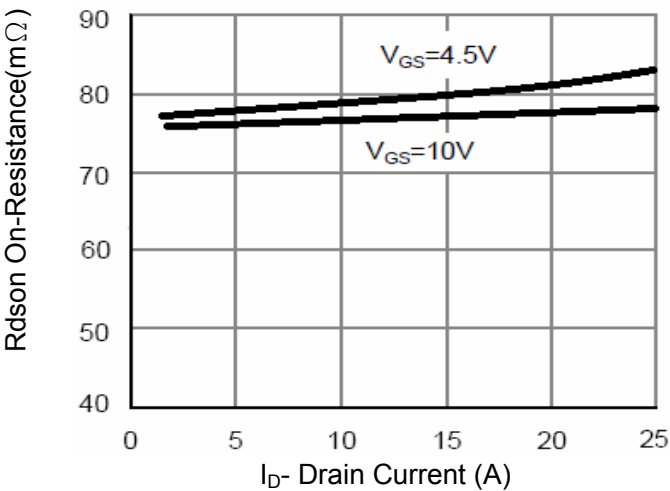


Figure 3 Rdson- Drain Current

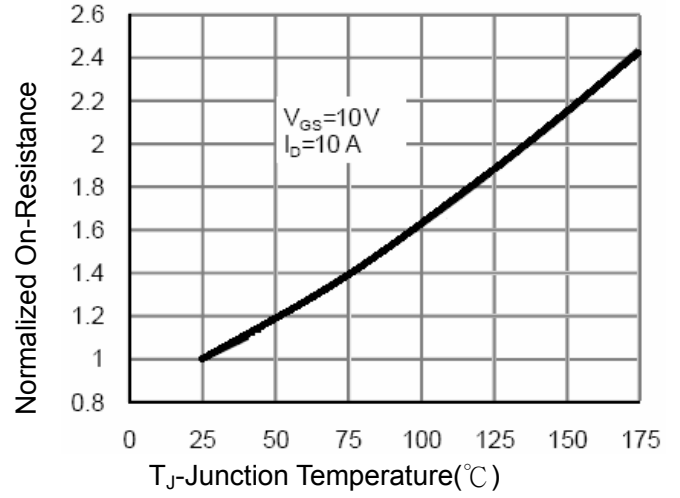


Figure 4 Rdson-Junction Temperature

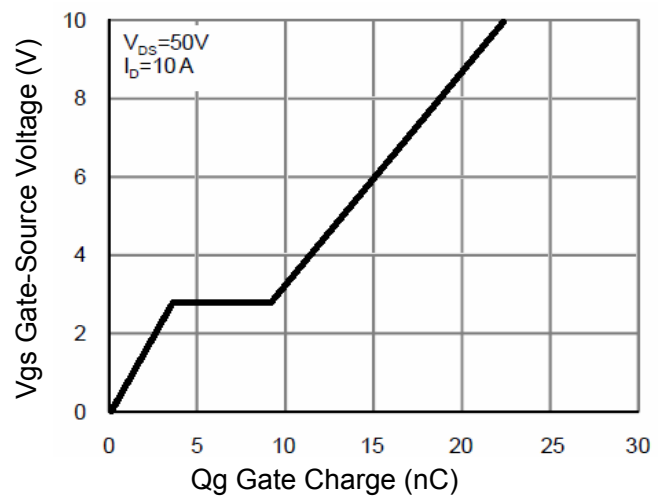


Figure 5 Gate Charge

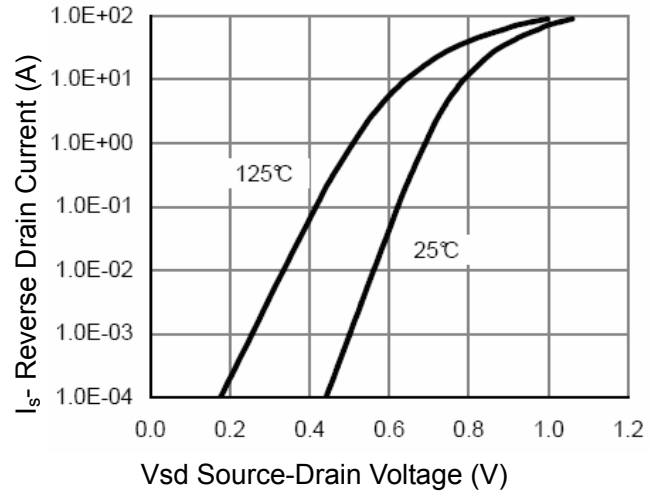


Figure 6 Source- Drain Diode Forward

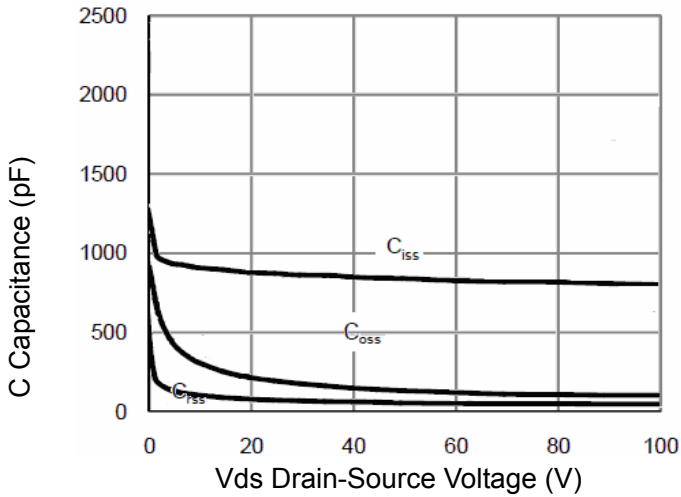


Figure 7 Capacitance vs Vds

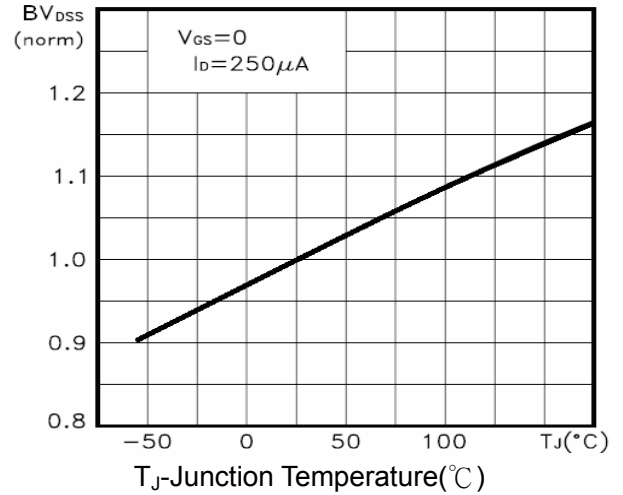


Figure 9  $BV_{DSS}$  vs Junction Temperature

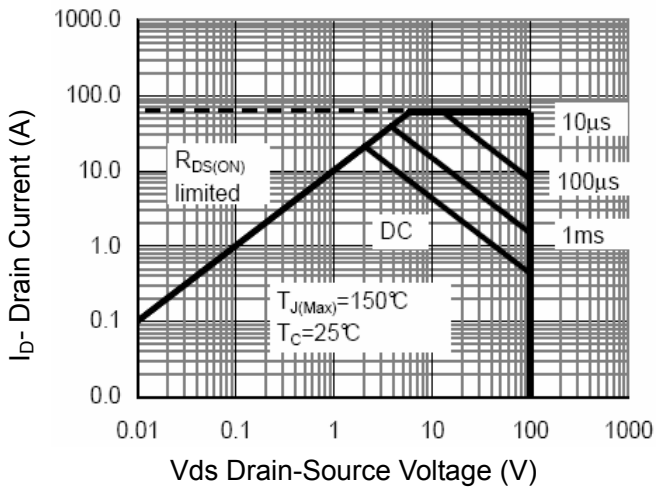


Figure 8 Safe Operation Area

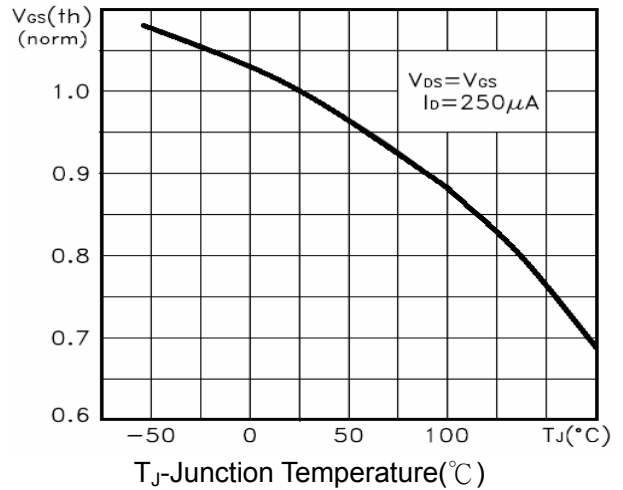


Figure 10  $V_{GS(th)}$  vs Junction Temperature

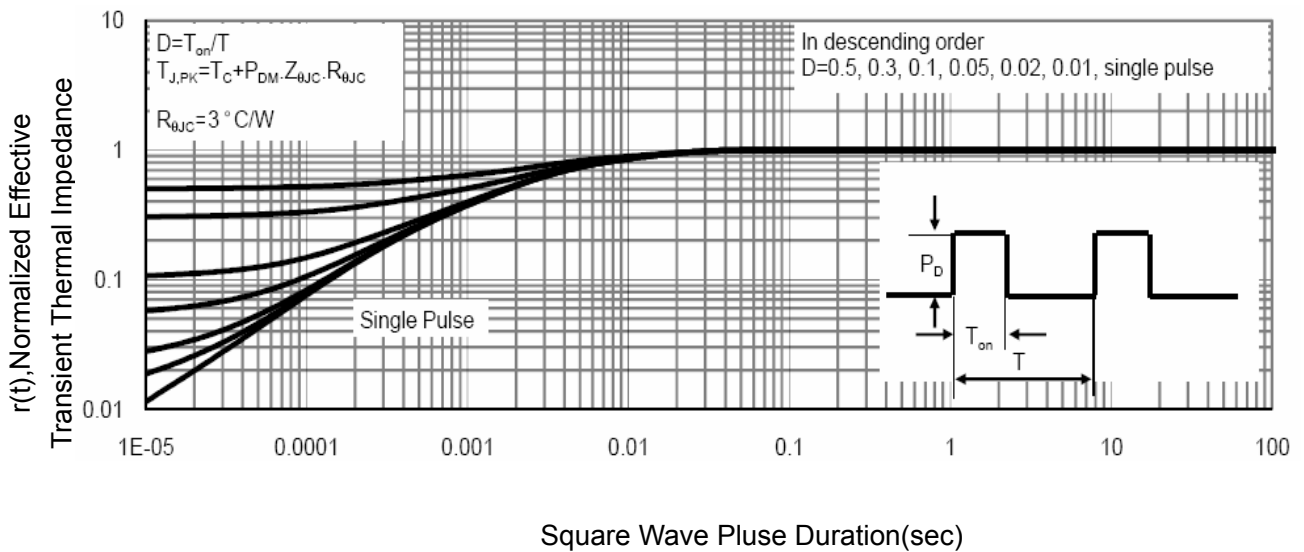
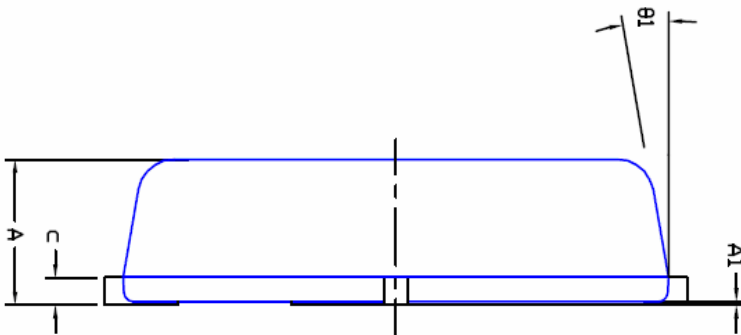
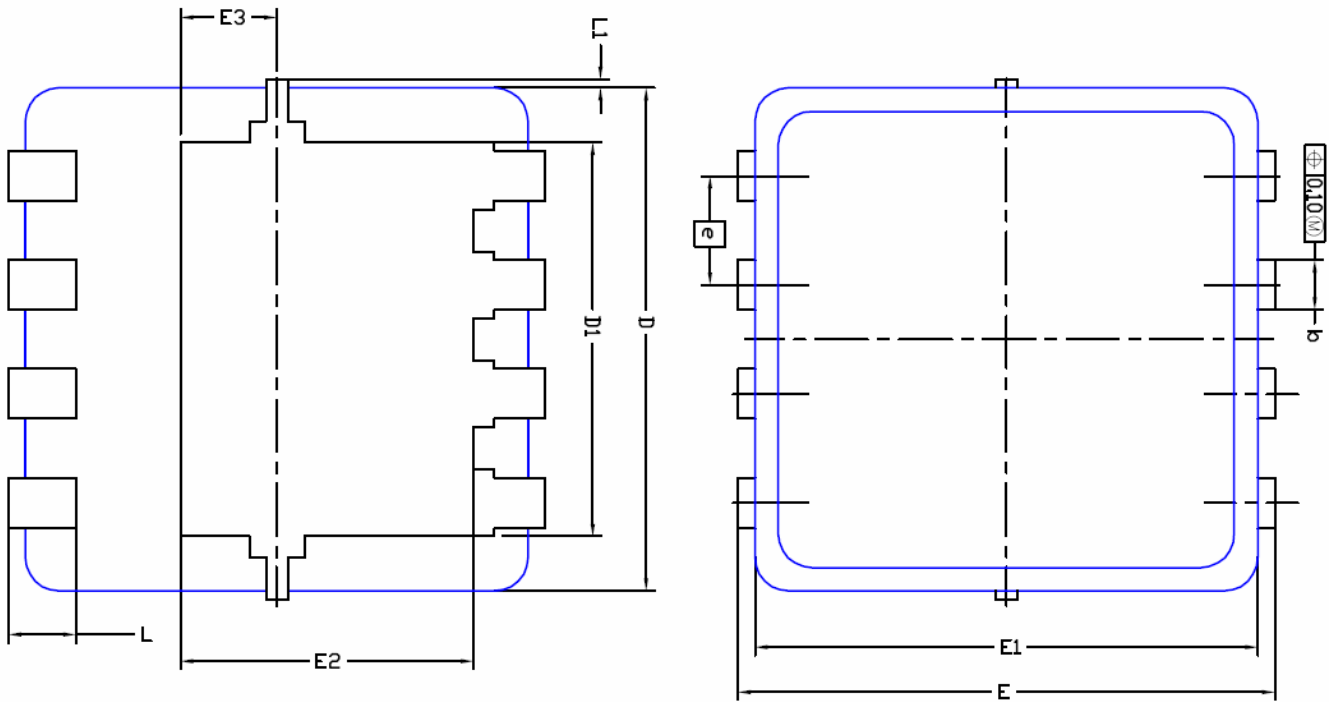


Figure 11 Normalized Maximum Transient Thermal Impedance

## DFN3X3 EP Package Information



DIM.	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.80	0.900	0.0276	0.0315	0.0354
A1	0.00	---	0.05	0.000	---	0.002
b	0.24	0.30	0.35	0.009	0.012	0.014
c	0.10	0.152	0.25	0.004	0.006	0.010
D	3.00 BSC			0.118 BSC		
D1	2.35 BSC			0.093 BSC		
E	3.20 BSC			0.126 BSC		
E1	3.00 BSC			0.118 BSC		
E2	1.75 BSC			0.069 BSC		
E3	0.575 BSC			0.023 BSC		
e	0.65 BSC			0.026 BSC		
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
L1	0	---	0.100	0	---	0.004
theta1	0°	10°	12°	0°	10°	12°