

## Very High PSRR Low Noise 300mA RF LDO

### General Description

The HM1134BXX2DR family of low-dropout (LDO), low-power linear regulators offers very high power supply rejection ratio (PSRR) while maintaining very low 40 $\mu$ A ground current, suitable for RF applications. The family uses an advanced CMOS process and a PMOSFET pass device to achieve fast start-up, very low noise, excellent transient response, and excellent PSRR performance. The HM1134BXX2DR is stable with a 1.0 $\mu$ F ceramic output capacitor, and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 2% over all load, line, process, and temperature variations. It is fully specified from  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  and is offered in a small DFN4 package, which is ideal for small form factor portable equipment such as wireless handsets and PDAs.

The HM1134BXX2DR is available in standard fixed output voltages of 1.2V (HM1134B122DR), 1.5V (HM1134B152DR), 1.8V (HM1134B182DR), 2.5V (HM1134B252DR), 2.8 (HM1134B282DR), 3.0V (HM1134B302DR), 3.3V (HM1134B332DR), and custom voltage options (50mV step options between 0.8V and 5.0V are available upon request).

### Features

- Wide Input Voltage Range: 1.4V to 6.0V
- Up to 300mA Load Current
- Standard Fixed Output Voltage Options: 1.2V, 1.5V, 1.8V, 2.5V, 2.8V, 3.0V, and 3.3V
- Other Output Voltage Options Available on Request
- Very Low  $I_Q$ : 36 $\mu$ A
- Ultra Low Dropout: 190mV at 300mA Load
- Very High PSRR: 80db at 100Hz
- Ultra Low Noise: 45 $\mu$ Vrms at 1.2V output
- Ultra-Fast Start-Up Time: 25 $\mu$ s
- Excellent Load/Line Transient Response
- Line Regulation: 0.03% typical
- Package: DFN4(1\*1)( HM1134BXX2DR)

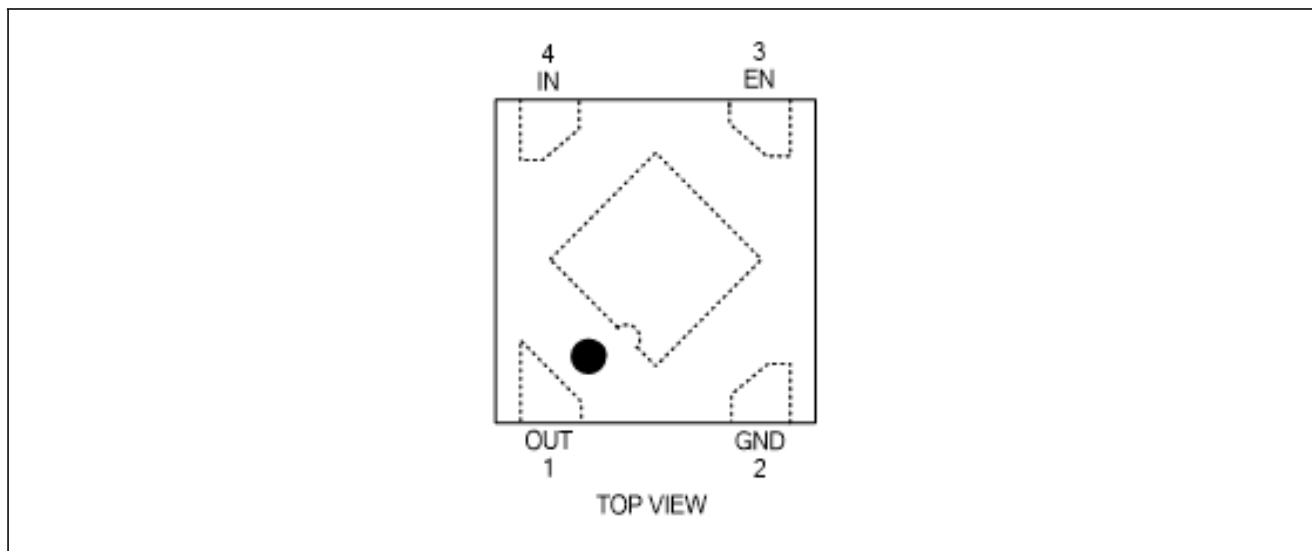
## Applications

Smart Phones and Cellular Phones  
 PDAs  
 MP3/MP4 Player  
 Digital Still Cameras  
 Portable instruments

## Mark Specification

Part No.	Marking	V <sub>OUT</sub>	Auto Discharge Function
HM1134B122DR	A1	1.2V	Y
HM1134B152DR	B1	1.5V	Y
HM1134B182DR	C1	1.8V	Y
HM1134B252DR	F1	2.5V	Y
HM1134B282DR	D1	2.8V	Y
HM1134B302DR	G1	3.0V	Y
HM1134B332DR	E1	3.3V	Y

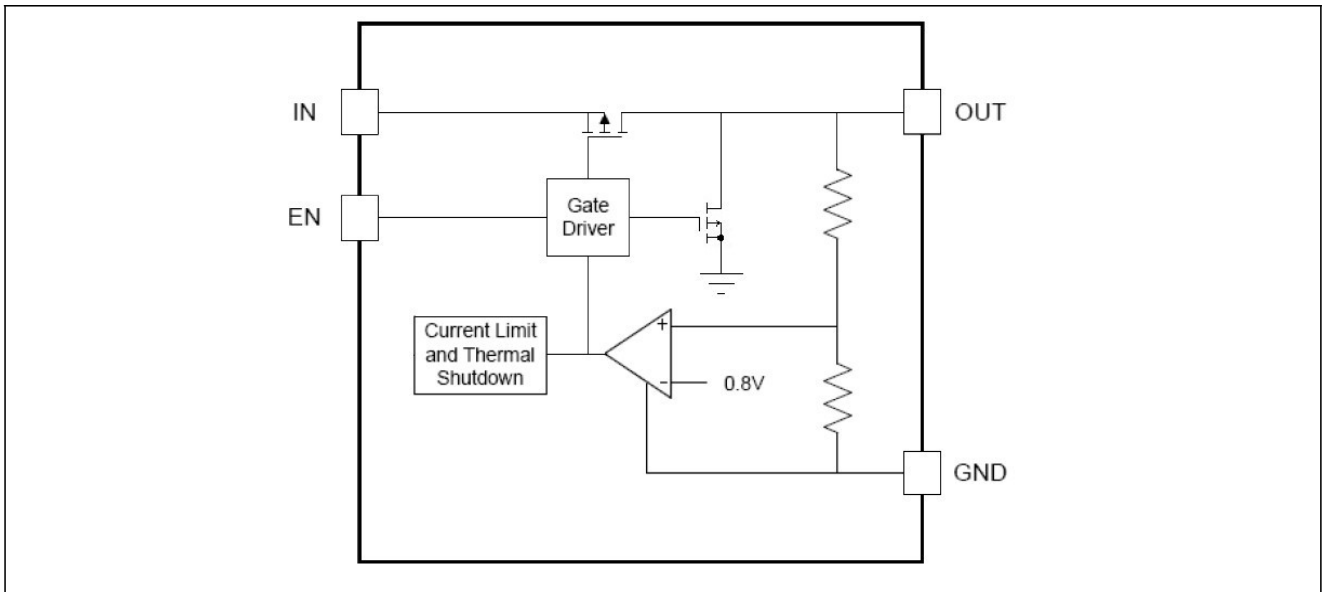
## Pin Configuration



## Pin Function

Pin No.	Pin Name	Pin Function
4	IN	Supply input pin. Must be closely decoupled to GND with a 1μF or greater ceramic capacitor
2	GND	Ground
3	EN	Enable control input, active high. Do not leave EN floating
1	OUT	Output pin. Bypass a 1μF ceramic capacitor from this pin to ground

## Block Diagram



## Functional Description

### Input Capacitor

A 1 $\mu$ F ceramic capacitor is recommended to connect between  $V_{IN}$  and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both  $V_{IN}$  and GND.

### Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from 1 $\mu$ F to 2.2 $\mu$ F, Equivalent Series Resistance (ESR) is from 5m $\Omega$  to 100m $\Omega$ , and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins.

### ON/OFF Input Operation

The HM1134BXX2DR is turned on by setting the EN pin high, and is turned off by pulling it low. If this feature is not used, the EN pin should be tied to IN pin to keep the regulator output on at all time.

### High PSRR and Low Noise

RF circuits such as LNA (low-noise amplifier), up/down-converter, mixer, PLL, VCO, and IF stage, require low noise and high PSRR LDOs. The temperature-compensated crystal oscillator circuit requires very high PSRR at RF power amplifier burst frequency. For instance, minimum 65dB PSRR at 217Hz is recommended for the GSM handsets.

In order to provide good audio quality, the audio power supply for hand-free, game, MP3, and multimedia applications in cellular phones, require low-noise and high PSRR at audio frequency range (20Hz-20kHz).

The HM1134BXX2DR, with PSRR of 80dB at 100Hz, is suitable for most of these applications that require high PSRR and low noise.

#### Ultra Fast Start-up

After enabled, the HM1134BXX2DR is able to provide full power in as little as tens of microseconds, typically 25µs. This feature will help load circuitry move in and out of standby mode in real time, eventually extend battery life for mobile phones and other portable devices.

#### Fast Transient Response

Fast transient response LDOs can also extend battery life. TDMA-based cell phone protocols such as Global System for Mobile Communications (GSM) have a transmit/receive duty factor of only 12.5 percent, enabling power savings by putting much of the baseband circuitry into standby mode in between transmit cycles. In baseband circuits, the load often transitions virtually instantaneously from 100µA to 100mA. To meet this load requirement, the LDO must react very quickly without a large voltage drop or overshoot — a requirement that cannot be met with conventional, general-purpose LDOs.

The HM1134BXX2DR's fast transient response from 0 to 150mA provides stable voltage supply for fast DSP and GSM chipset with fast changing load.

#### Low Quiescent Current

Cellular phone baseband internal digital circuits typically operate all the time. That requires LDO stays on at all times. However, in the standby mode, the microprocessor consumes only around 100~300µA. Since the phone stays in standby for the longest percentage of time, using a 40µA quiescent current LDO, instead of 100µA, saves 60µA and can substantially extends the battery standby time.

The HM1134BXX2DR, consuming only around 40µA for all input range and output loading, provides great power saving in portable and low power applications.

#### Current Limit Protection

When output current at the OUT pin is higher than current limit threshold or the OUT pin is short-circuit to GND, the current limit protection will be triggered and clamp the output current to approximately 500mA to prevent over-current and to protect the regulator from damage due to overheating.

#### Thermal Shutdown Protection

Thermal protection disables the output when the junction temperature rises to approximately +155°C, allowing the device to cool down. When the junction temperature reduces to approximately +130°C the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

#### Absolute Maximum Ratings

Parameter	Rating	Unit
IN Voltage	-0.3 to 6.5	V
Other Pin Voltage	-0.3 to $V_{IN}+0.3$	V
Maximum Load Current	500	mA
Operating Junction Temperature	-40 to 125	°C
Storage Temperature	-65 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

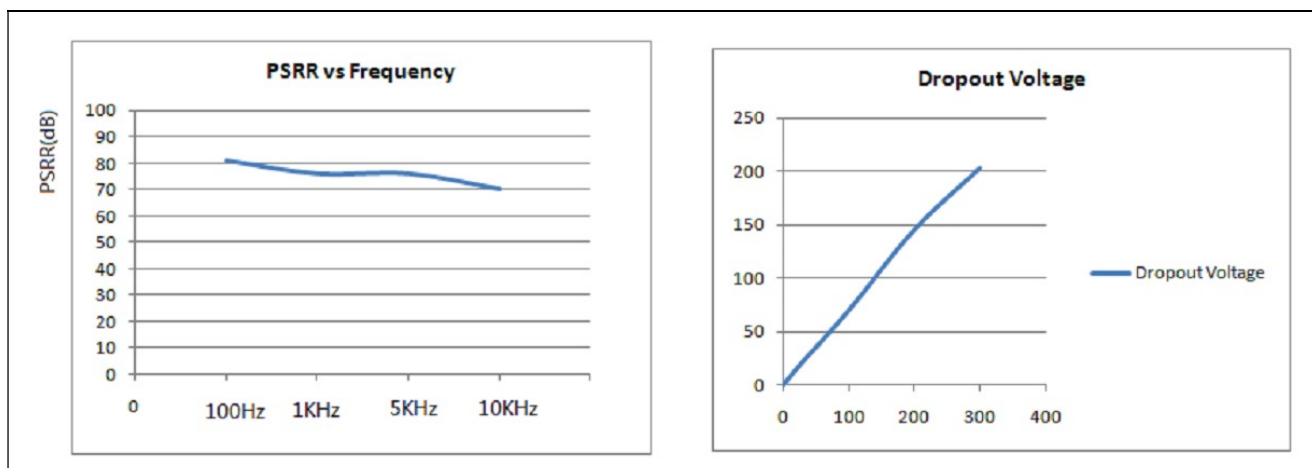
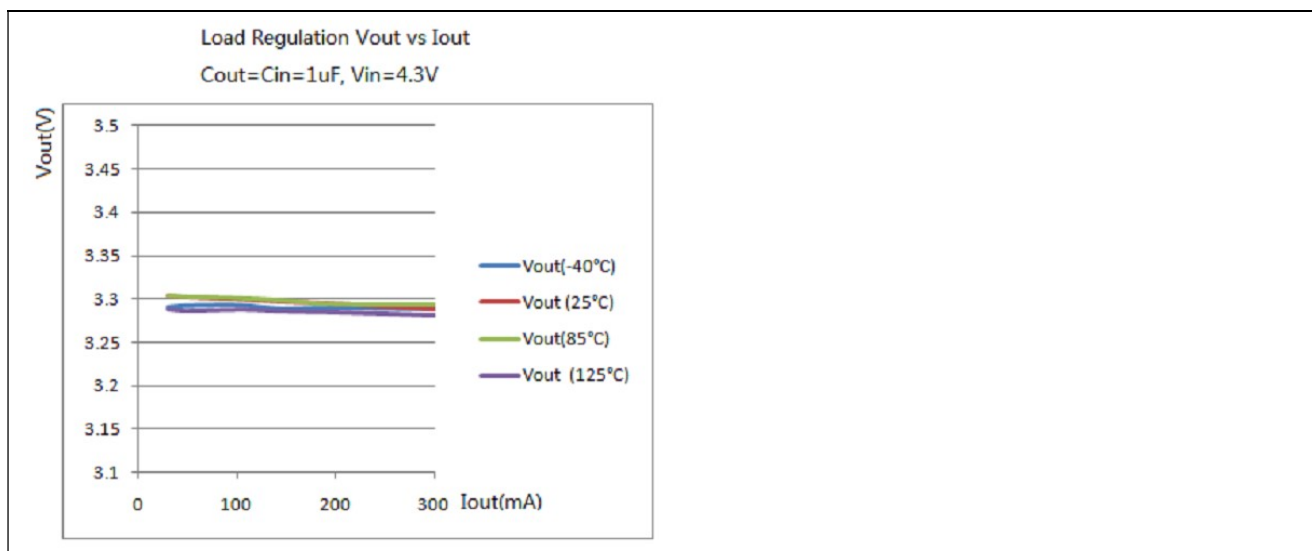
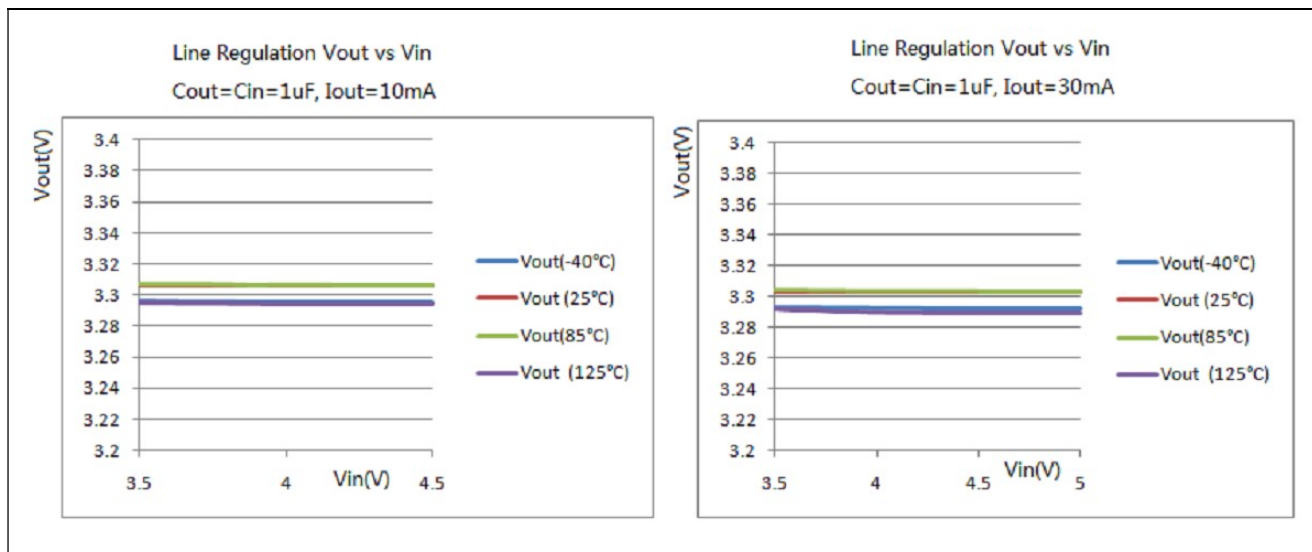
## Electrical Characteristics

( $V_{IN}=V_{EN}=3.6V$ ,  $T_A=25^{\circ}C$  unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Operation Range	$V_{IN}$		1.4		6.0	V
Dropout Voltage		$V_{OUT} \geq 2.8V$ , $I_{OUT} = 300mA$		230		mV
DC Supply Quiescent Current	$I_{Q\_ON}$	Active mode: $V_{EN}=V_{IN}$		36	49	$\mu A$
DC Supply Shutdown Current	$I_{Q\_OFF}$	$V_{EN}=0V$		0.01	1	$\mu A$
Regulated Output Voltage	$V_{OUT}$	$I_{OUT}=1mA$ , $-40^{\circ}C \leq T_A \leq 85^{\circ}C$	-2		2	%
Output Voltage Line Regulation		$V_{IN} = V_{OUT} + 1V$ to $5.5V$ , $I_{OUT} = 10mA$		0.03	0.2	%
Output Voltage Load Regulation		$I_{OUT}$ from $0mA$ to $300mA$		0.2	0.7	%
Soft-start Time		From Enable to Power On		25		$\mu s$
Current Limit			300			mA
Maximum Output Current	$V_{IN} < 4.4V$	$V_{OUT} < 2V$	150			mA
		$2.8V > V_{OUT} \geq 2V$	250			
		$V_{OUT} \geq 2.8V$	300			
Power Supply Rejection Ratio	PSRR	$f=100Hz$ , $C_{OUT}=1\mu F$ , $I_{OUT}=20mA$		80		dB
Power Supply Rejection Ratio	PSRR	$f=1kHz$ , $C_{OUT}=1\mu F$ , $I_{OUT}=20mA$		75		dB
Power Supply Rejection Ratio	PSRR	$f=10kHz$ , $C_{OUT}=1\mu F$ , $I_{OUT}=30mA$		65		dB
Output Noise		$10Hz$ to $100kHz$ , $I_{OUT} = 200mA$ , $V_{OUT}=2.8V$ , $C_{OUT} = 1\mu F$		70		$\mu V_{RMS}$
		$10Hz$ to $100kHz$ , $I_{OUT} = 200mA$ , $V_{OUT}=1.2V$ , $C_{OUT} = 1\mu F$		45		
EN Low Threshold					0.3	V
EN High Threshold			1.5			V
EN Pin Input Current	$I_{EN}$			0	0.1	$\mu A$
Over-temperature Shutdown Threshold				155		$^{\circ}C$
Over-temperature Shutdown Hysteresis				20		$^{\circ}C$

Note: Production test at  $+25^{\circ}C$ . Specifications over the temperature range are guaranteed by design and characterization

## Typical Performance Curves



## Load Transient Response

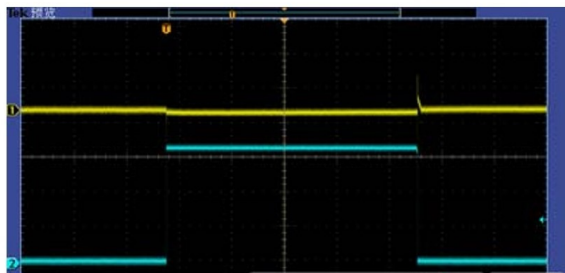
VIN=4.2V, VOUT=3.3V, CIN=COUT=1uF,

IOUT=10mA to 160mA to 10mA (Rise/Fall time=500ns)

CH1: VOUT, 50mV/Div, DC Offset=3.3V

CH2: IOUT, 50mA/Div DC

TIME: 20ms/Div



## Load Transient Response

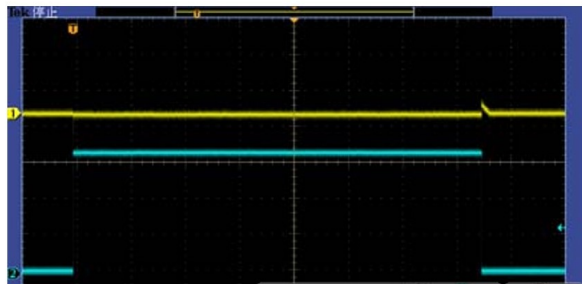
VIN=4.2V, VOUT=3.3V, CIN=COUT=1uF,

IOUT=10mA to 80mA to 10mA (Rise/Fall time=500ns)

CH1: VOUT, 100mV/Div, DC Offset=3.3V

CH2: IOUT, 25mA/Div DC

TIME: 10ms/Div



## Line Transient Response

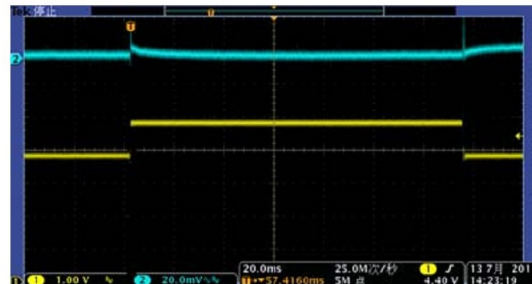
VIN=3.8V to 4.8V to 3.8V (Rise/Fall time=500ns),

VOUT=3.3V, CIN=COUT=1uF, IOUT=100mA

CH2: VOUT, 20mV/Div DC Offset=3.3V

CH1: VIN, 2V/Div, DC Offset=3.8V

TIME: 20ms/Div





## Line Transient Response

VIN=3.8V to 4.8V to 3.8V (Rise/Fall time=500ns),

VOUT=3.3V, CIN=COUT=1uF, IOUT=50mA

CH2: VOUT, 20mV/Div DC Offset=3.3V

CH1: VIN, 2V/Div, DC Offset=3.8V

TIME: 20ms/Div



## Line Transient Response

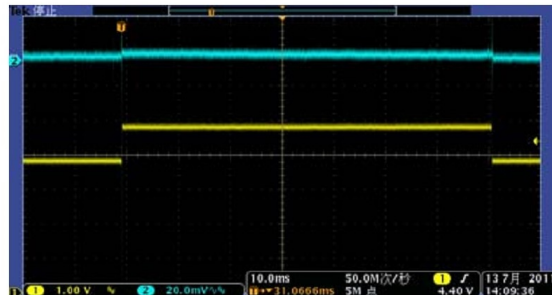
VIN=3.8V to 4.8V to 3.8V (Rise/Fall time=500ns),

VOUT=3.3V, CIN=COUT=1uF, IOUT=10mA,

CH2: VOUT, 20mV/Div, DC Offset=3.3V

CH1: VIN, 2V/Div, DC Offset=3.8V

TIME: 20ms/Div



## Exiting Shutdown

VIN=4.2V, VOUT=3.3V, CIN=COUT=1uF,

IOUT=10mA

CH1: EN, 5V/Div, DC

CH2: VOUT, 1V/Div DC

TIME: 40us/Div



## Entering Shutdown

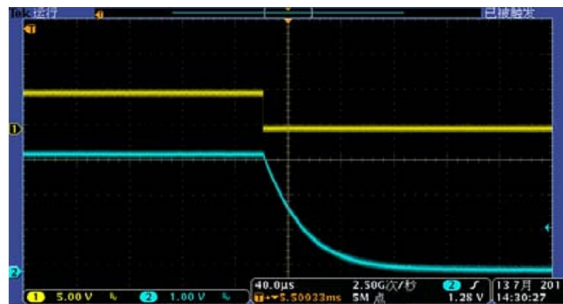
VIN=4.2V, VOUT=3.3V, CIN=COUT=1uF,

IOUT=10mA

CH1: EN, 5V/Div, DC

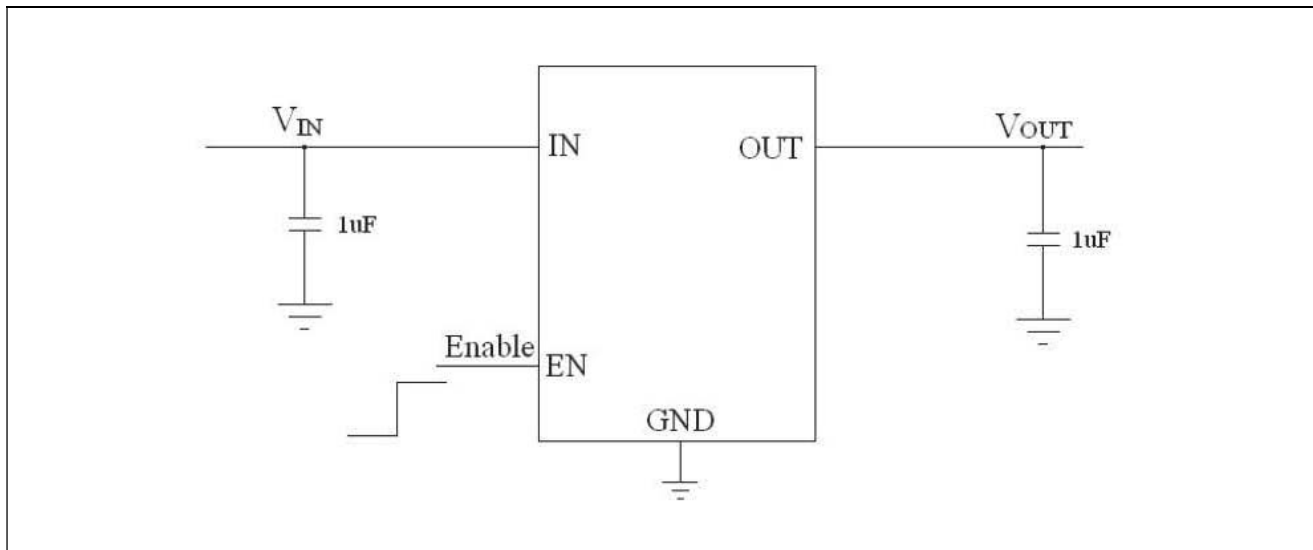
CH2: VOUT, 1V/Div DC

TIME: 40us/Div





## Application Circuits



## Package Dimension

DFN4 (1\*1)

