

HM8243

3 Cell Li-Ion/Polymer Battery Pack Protection IC

Features

- Overcharge protection
 - Threshold from 4.175V to 4.350V, 25mV steps, $\pm 25\text{mV}$ accuracy
- Over discharge protection
 - Threshold from 2.300V to 3.000V, 25mV steps, $\pm 80\text{mV}$ accuracy
- Excess current protection
 - Excess current 1:
Threshold from 0.030V to 0.100V, 10mV steps, $\pm 5\text{mV}$ accuracy
 - Excess current 2:
Threshold from 0.060V to 0.200V, 20mV steps, $\pm 5\text{mV}$ accuracy
 - Short circuits protection:
Threshold from 0.090V to 0.600V, 30mV steps, $\pm 10\text{mV}$ accuracy
- Charge and discharge over temperature protection
- Automatic recovery after excess current protection
- Ultra low power dissipation
 - Normal working $15\mu\text{A}$ (25°C)
 - Sleep mode $5\mu\text{A}$ (25°C)
- Package type: SSOP16 and SOP16

Applications

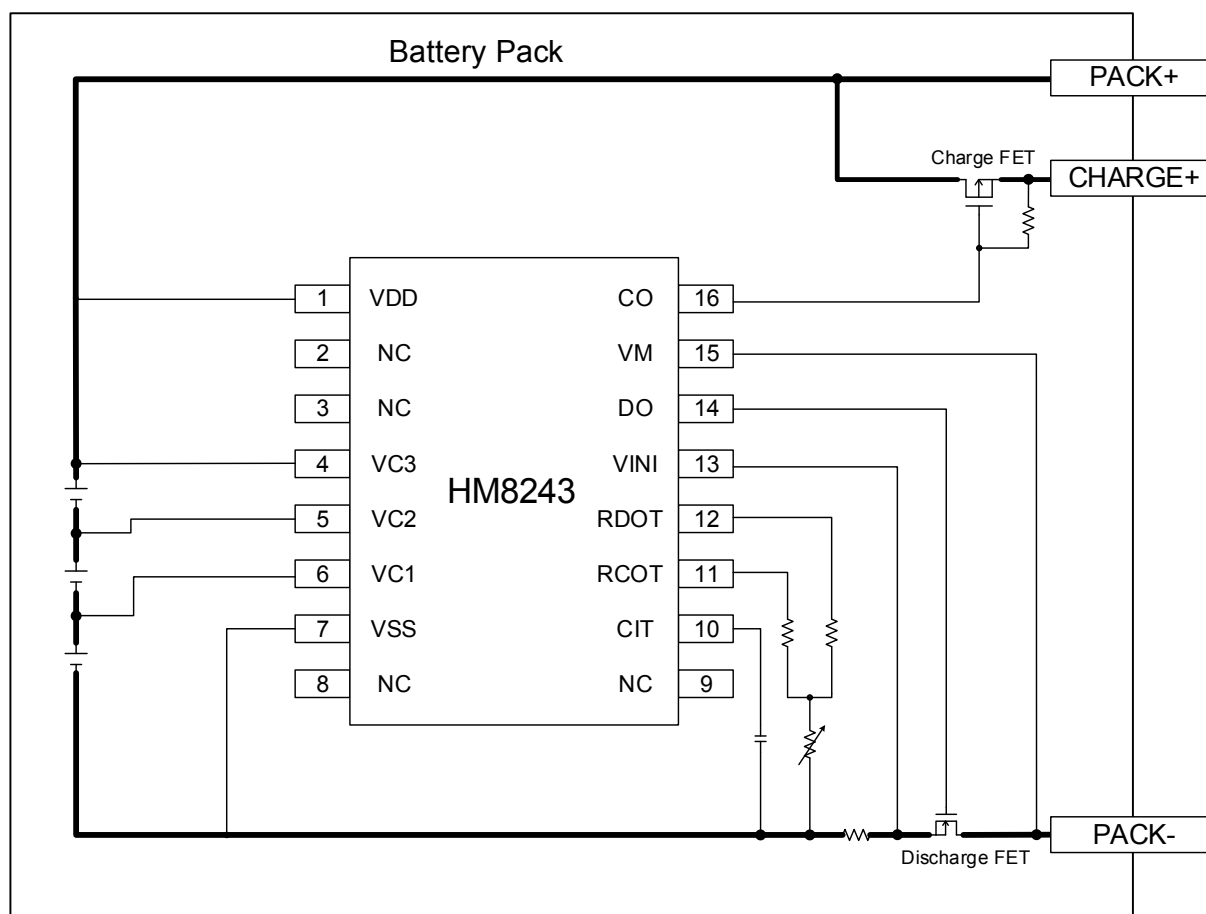
- Power tools
- E-bike
- Backup power supply
- Other lithium-ion or lithium polymer battery packs

General Description

The HM8243 series products are highly integrated protection ICs for 3 lithium-ion and lithium polymer battery packs connected in series.

HM8243 provides complete protection for battery pack by measuring the voltage, current and temperature.

Typical Application



Product Name

HM8243 X X X

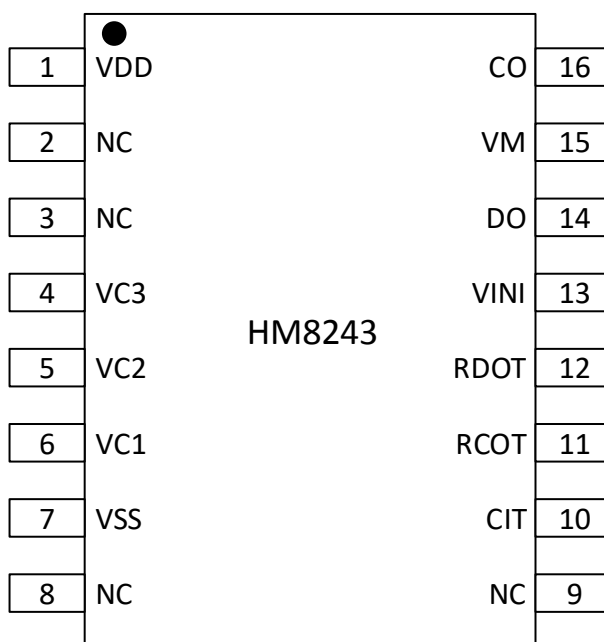
Package type, S: SSOP16; U: SOP16
Parameter option, from A to Z
Battery type, L: Lithium T: Charge low temperature protection

Ordering Information

| PART | OVER CHARGE DETECTION VOLTAGE [Voc] | OVER CHARGE RELEASE VOLTAGE [Vocr] | OVER DISCHARGE DETECTION VOLTAGE [Vod] | OVER DISCHARGE RELEASE VOLTAGE [Vodr] | DISCHARGE OVERCURRENT DETECTION VOLTAGE1 [Vec1] | DISCHARGE OVERCURRENT DETECTION VOLTAGE2 [Vec2] | SHORT CIRCUIT DETECTION VOLTAGE [Vshr] | CHARGE LOW TEMPERATURE PROTECTION |
|-----------|---|--|--|---|---|---|--|--|
| HM8243LAU | 4.200V | 4.100V | 2.700V | 3.000V | 0.050V | 0.100V | 0.250V | NO |
| HM8243LB | 4.250V | 4.150V | 2.700V | 3.000V | 0.100V | 0.200V | 0.500V | NO |
| HM8243LB | 4.250V | 4.150V | 2.700V | 3.000V | 0.100V | 0.200V | 0.500V | NO |
| HM8243LJ | 4.225V | 4.125V | 2.700V | 3.000V | 0.100V | 0.200V | 0.500V | NO |
| HM8243LJ | 4.225V | 4.125V | 2.700V | 3.000V | 0.100V | 0.200V | 0.500V | NO |
| HM8243LL | 4.200V | 4.100V | 2.500V | 3.000V | 0.100V | 0.200V | 0.500V | NO |
| HM8243TJ | 4.225V | 4.125V | 2.700V | 3.000V | 0.100V | 0.200V | 0.500V | YES |

Pin Configuration

HM8243 (TOP VIEW)



Pin Descriptions

| PIN | NAME | DESCRIPTION |
|-----|------|---|
| 1 | VDD | Power supply, connect to the most positive voltage |
| 2 | NC | No connection |
| 3 | NC | No connection |
| 4 | VC3 | Voltage measurement input of the 3 rd cell |
| 5 | VC2 | Voltage measurement input of the 2 nd cell |
| 6 | VC1 | Voltage measurement input of the 1 st cell |
| 7 | VSS | Ground |
| 8 | NC | No connection |
| 9 | NC | No connection |
| 10 | CIT | Excess current delay set pin |
| 11 | RCOT | Charge over temperature resistor connect point |
| 12 | RDOT | Discharge over temperature resistor connect point |
| 13 | VINI | Excess current detect input |
| 14 | DO | Over-discharge protection output |
| 15 | VM | P- voltage detect input |
| 16 | CO | Overcharge protection output, open-drain output |

Note: The pin arrangements of SOP16 and SSOP16 package are same.

Absolute Maximum Ratings

| | | VALUE | | UNITS |
|----------------------------------|-------------------------|---------|---------|-------|
| | | MIN | MAX | |
| PIN voltage range respect to VSS | VDD, VM, CO | -0.3 | 30 | V |
| PIN voltage range respect to VSS | RCOT, RDOT, CIT | -0.3 | 6 | V |
| PIN voltage range | VC1, VC2, VC3, DO, VINI | VSS-0.3 | VDD+0.3 | V |
| Operation Temperature | T1 | -30 | 85 | °C |
| Storage Temperature | T2 | -40 | 125 | °C |

Caution:

Stresses beyond "Absolute Maximum Ratings" condition may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------|-------------------------------|------------|-----|-----|------|-------|
| VDD Input Voltage Range | V_{DD} | | 4 | | 13.5 | V |
| VCELL Input Voltage Range | V_{CELL} | | 0 | | 4.5 | V |
| PIN Input Voltage Range | $V_{CIT}, V_{RCOT}, V_{RDOT}$ | | 0 | | 5 | V |

Electrical Characteristics

Operation under 25°C unless otherwise specified

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---------------|--|---------------------|-----------|---------------------|-------|
| POWER SUPPLY | | | | | | |
| Operation Current | I_{OPR} | VC1=VC2=VC3= 3.7V | | 15 | 20 | μA |
| Sleep Current | I_{SLEEP} | VC1=VC2=VC3= 2.0V | | 5 | | μA |
| VOLTAGE/TEMPERATURE DETECT AND PROTECTION THRESHOLD | | | | | | |
| Over charge Threshold | V_{OC}^{*1} | VC1=VC2= 3.7V Sweep VC3 from 3.7V to 4.5V | V_{OC-} 0.025 | V_{OC} | V_{OC+} 0.025 | V |
| OC release threshold | V_{OCR} | VC1=VC2= 3.7V Sweep VC3 from 4.5V to 3.7V | V_{OCR-} 0.050 | V_{OCR} | V_{OCR+} 0.050 | V |
| Over Discharge Threshold | V_{OD} | VC1=VC2= 3.7V Sweep VC3 from 3.7V to 2.0V | V_{OD-} 0.080 | V_{OD} | V_{OD+} 0.080 | V |
| OD Release Threshold | V_{ODR} | VC1=VC2= 3.7V Sweep VC3 from 2.0V to 3.7V | V_{ODR-} 0.100 | V_{ODR} | V_{ODR+} 0.100 | V |

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------------|----------------|--|-----------------|-----------|-----------------|-------|
| Excess Current 1 Threshold | V_{EC1} | VC1=VC2=VC3= 3.7V Sweep VINI from 0V to 0.15V | $V_{EC1}-0.005$ | V_{EC1} | $V_{EC1}+0.005$ | V |
| Excess Current 2 Threshold | V_{EC2} | VC1=VC2=VC3= 3.7V Sweep VINI from 0V to 0.3V | $V_{EC2}-0.005$ | V_{EC2} | $V_{EC2}+0.005$ | V |
| Short Circuits Protection | V_{SHR} | VC1=VC2=VC3= 3.7V Sweep VINI from 0V to 0.6V | $V_{SHR}-0.010$ | V_{SHR} | $V_{SHR}+0.010$ | V |
| Charge Over Temperature | T_{COT}^{*2} | VDD=10.8V | $T_{COT}-2$ | T_{COT} | $T_{COT}+2$ | °C |
| COT Release | T_{COTR} | | | 5 | | °C |
| Discharge Over Temperature | T_{DOT}^{*2} | VDD=10.8V | $T_{DOT}-2$ | T_{DOT} | $T_{DOT}+2$ | °C |
| DOT Release | T_{DOTR} | | | 5 | | °C |
| ACTION DELAY | | | | | | |
| Overcharge Delay | T_{OC} | VC1=VC2= 3.7V Sweep VC3 from 3.7V to 4.5V | $0.5^{*}T_{OC}$ | T_{OC} | $1.5^{*}T_{OC}$ | s |
| Overcharge Reset Delay | T_{RESET} | | | 20 | | ms |
| Overcharge Release Delay | T_{OCR} | VC1=VC2= 3.7V Sweep VC3 from 4.5V to 3.7V | | 280 | | ms |
| Over Discharge Delay | T_{OD} | VC1=VC2= 3.7V Sweep VC3 from 3.7V to 2.0V | $0.5^{*}T_{OD}$ | T_{OD} | $1.5^{*}T_{OD}$ | s |
| Over Discharge Release delay | T_{ODR} | VC1=VC2= 3.7V Sweep VC3 from 2.0V to 3.7V | | 560 | | ms |
| Excess Current 1 Delay | T_{EC1} | CIT Capacitor 0.1μF | | 1 | | s |
| Excess Current 2 Delay | T_{EC2} | CIT Capacitor 0.1μF | | 100 | | ms |
| Short Protection Delay | T_{SHORT} | | | 280 | | μs |
| Excess Current Release Delay | T_{ECR}^{*3} | | | 280 | | ms |
| Load it Locked Release Delay | T_{LLR} | VC1=VC2=VC3= 3.7V VM<VDD/3 | | 280 | | ms |
| Sleep Delay | T_{SLP} | | | 30 | | s |
| COT Protection Delay | T_{COT} | | | 1 | | s |
| COT Release Delay | T_{COTR} | | | 1 | | s |
| DOT Protection Delay | T_{DOT} | | | 1 | | s |
| DOT Release Delay | T_{DOTR} | | | 2 | | s |
| Open-wire Delay | T_{OW} | VCELL Capacitor 0.1μF | | 8 | | s |
| Open-wire Release Delay | T_{OWR} | | | 20 | | ms |
| 0V CHARGE FUNCTION | | | | | | |

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------------------|--------------------|-----------------------|-----|----------------------|-----|-------|
| 0V Charging Start Voltage | V _{0V} | | 1.5 | | | V |
| VM | | | | | | |
| VM/VSS internal resistance | R _{VMVSS} | | | 66 | | kΩ |
| PIN OUTPUT VOLTAGE | | | | | | |
| CO Logic Low Output | CO*4 | | | VSS | | V |
| DO Logic High Output | DO | V _{DD} >=11V | | 10 | | V |
| DO Logic High Output | | V _{DD} <11V | | V _{DD} -0.7 | | V |
| DO Logic Low Output | | | | VSS | | V |
| PIN DRIVE ABILITY | | | | | | |
| CO Output Drive Ability | CO | CO logic HIGH*4 | | -- | | μA |
| | | CO logic LOW | | 6 | | μA |
| DO Output Drive Ability | DO | DO logic HIGH | | 50 | | μA |
| | | DO logic LOW | | -150 | | μA |

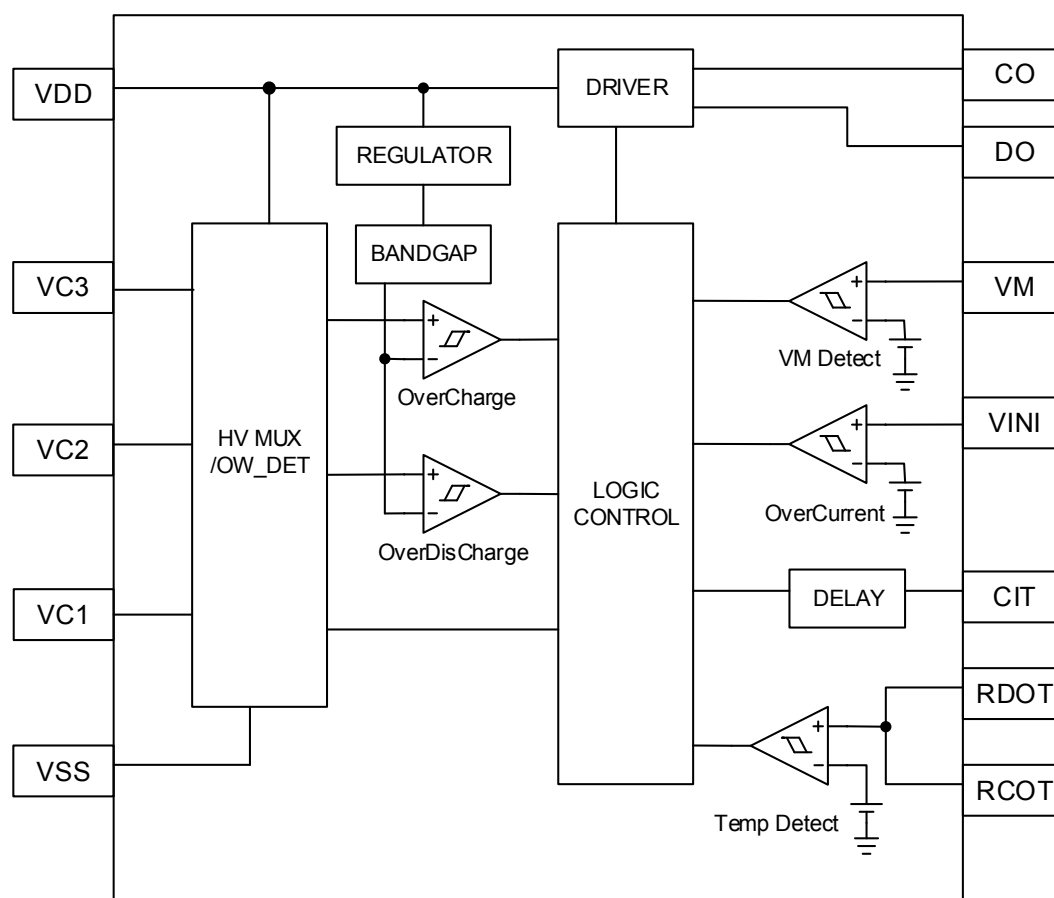
*1 Specified protection threshold is determined by device selection. Please refer to the selection guide table.

*2 Protection threshold is determined by the actual resistor net. Different charge and discharge over temperature protection threshold is only available for the different charge and discharge port application scheme.

*3 All the excess current (including EC1, EC2 and short) release delay time are 280ms.

*4 Logic high output of CO pin is High-Z.

Functional Block Diagram



Detailed Description

Normal State

All the battery voltages are between V_{OC} and V_{OD} , VINI is lower than the V_{EC1} , HM8243 works under the normal state.

Overcharge State

Any cell input voltage becomes higher than overcharge threshold voltage (V_{OC}) and stays longer than overcharge protection delay time (T_{OC}), CO outputs a high-resistance state to cut off the charging MOSFET, HM8243 enters over charge state. If, within T_{OC} , any cell voltage drops lower than V_{OC} but stays shorter than overcharge reset delay time (T_{RESET}) before rising up over V_{OC} again, this pink will be ignored. Otherwise, accumulated delay time of overcharge will be reset.

The overcharge protection state release when:

All cell voltages is less than the overcharge release threshold (V_{OCR}) and stays longer than the release delay time (T_{OCR}).

Over Discharge State

Any cell input voltage becomes lower than over discharge threshold voltage (V_{OD}) and stays longer than over discharge protection delay time (T_{OD}), DO outputs a logic low voltage to cut off the discharging MOSFET, HM8243 enters over discharge state.

The over discharge protection state releases when:

All cell voltages is high than the over discharge release threshold (V_{ODR}) and stays longer than the release delay time (T_{OCR}), and, VM lower than the $VDD/3$.

Over Discharge Protection Locking State

Sometimes, HM8243 enters the over discharge protection with a load. In this condition, if all cell voltages are higher than over discharge release Threshold (V_{ODR}) and stays longer than the release delay time (T_{ODR}), IC will enter over discharge protection locking state. DO keeps logic low output even if the cell voltage is higher than release threshold. (V_{ODR}).

The protection locking state release when:

VM lower than the $VDD/3$, and stays longer than the release delay time (T_{LLR}).

Sleep State

When HM8243 already entered over discharge state and stays longer than sleep delay (T_{SLP}), HM8243 will enter sleep state. DO keeps logic low voltage to cut off the discharge MOSFET.

The sleep state release when:

All cell voltages are high than the over discharge release threshold (V_{ODR}) and stays longer than the release delay time (T_{OCR}), and, VM is lower than the $VDD/3$.

Excess Current State

HM8243 embedded 3 level excess current protection, excess current 1, excess current 2 and short circuits.

All the protection mechanism and sequence is all the same. Take EC1 for example.

Discharging current is vary with the external load, when the voltage drop on current sense resistor is bigger than excess current protection threshold (V_{EC1}) and stays longer than the delay time (T_{EC1}), DO outputs a logic low voltage to cut off the discharging MOSFET, HM8243 enters the excess current protection state.

The excess current protection state releases when:

VM lower than the $VDD/3$ and stays longer than the release delay time (T_{ECR})

0V Charge

HM8243 allows charging a 0V battery. If VDD is less than 0V charge start voltage V_{0V} , and we connect a charger which output voltage higher than MOSFET turn-on threshold, 0V battery is charged.

Delay Time Setting

Delay time is the interval between the protection threshold triggered and CO/DO output voltage changed. The delay time of excess current 1 and excess current 2 are all configured by the external capacitors.

Over Temperature Setting

When the voltage of COT and DOT achieves the internal compare threshold, charging over temperature or discharging over temperature protection triggered.

While the temperature decreases, and the difference is bigger than the release hysteresis (T_{COR} or T_{DOR}), and stays longer than the release delay time (T_{CORT} or T_{DORT}), over temperature protection releases.

Over temperature protection release integrates a load detection function. Protection state will be locked until the external load is removed.

Threshold setting steps:

1. Choose NTC first
2. Define the charging over temperature protection threshold, for example, 50°C
3. Look up the NTC Resistor-Temperature table or curve, find out the resistor value corresponding to 50°C , for example, $35\text{k}\Omega$
4. Employ a same value normal resistor connect to RCOT pin
5. Discharging over temperature setting use the same method, but the normal resistor connect to the RDOT pin
6. Detailed circuits refer to fig4. Choose the resistor net to match the over temperature function.

One NTC for different over temperature protection threshold in charge and discharge state is only available for different charge and discharge port application. If use the same charge and discharge port, RCOT and RDOT must be set to the same value.

Open-wire Detection

Each wire connected between the battery cell and IC will be monitored.

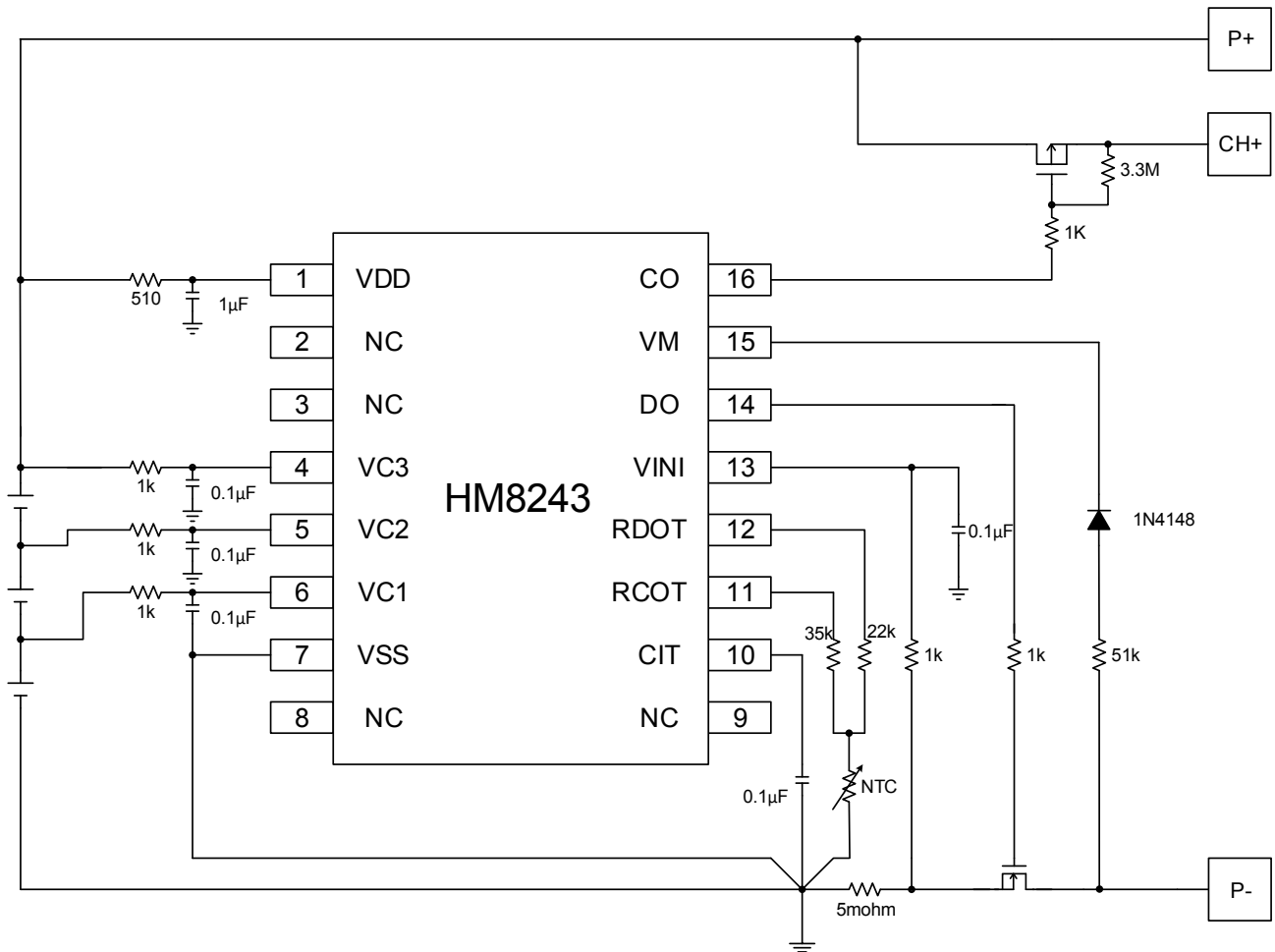
When the wire disconnects and maintains (T_{OW}) time, IC will enter to the open-wire protection state.

CO outputs a high-level voltage to cut off the charge loop. DO outputs a logic low voltage to cut off the discharging MOSFET.

Open-wire protection will release when all wires reconnect and stay longer than the release delay time.

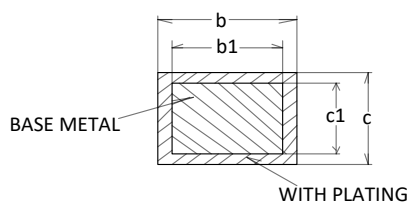
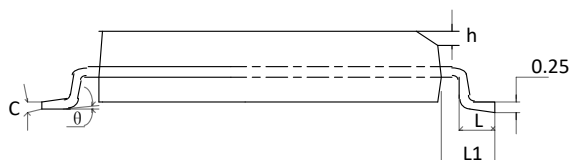
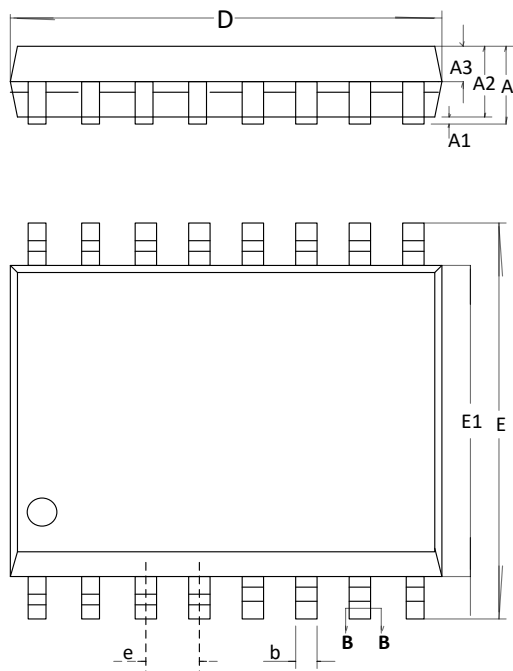
Open-wire protection release integrates a load detection function. Protection state will be locked until the external load is removed.

Reference Schematic



Package Information

SSOP16 Package

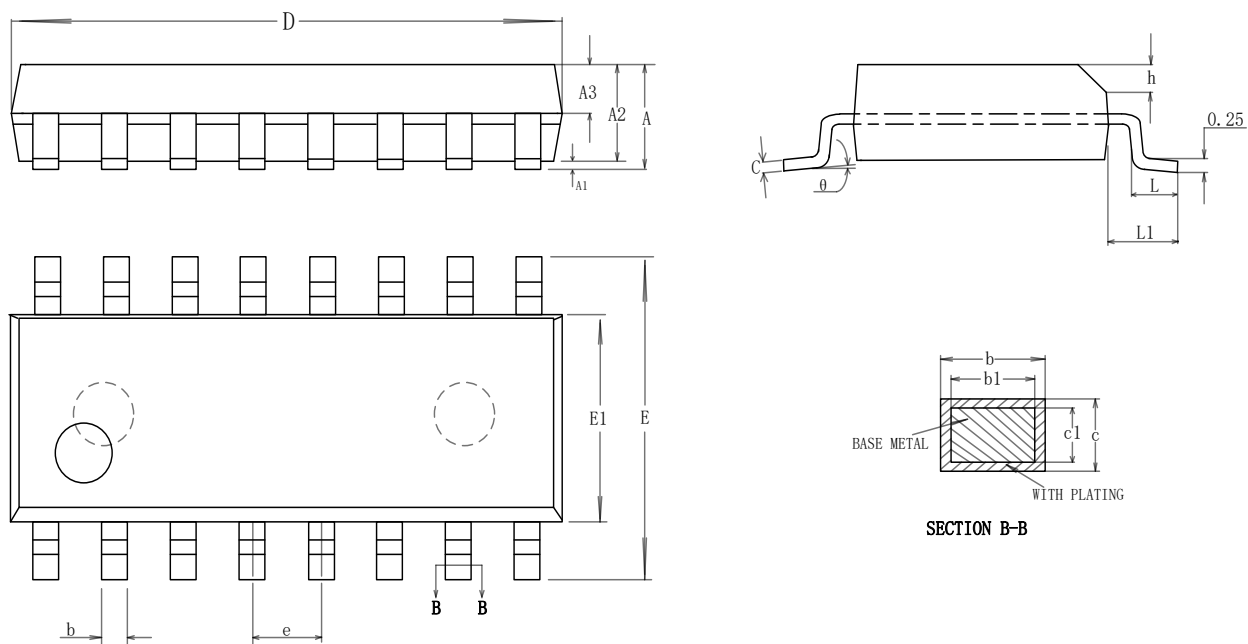


SECTION B-B

| SYMBOL | MILLIMETER | | |
|--------|------------|-------|-------|
| | MIN | NOM | MAX |
| A | ---- | ---- | 1.75 |
| A1 | 0.10 | ---- | 0.225 |
| A2 | 1.30 | 1.40 | 1.50 |
| A3 | 0.50 | 0.60 | 0.70 |
| b | 0.24 | ---- | 0.30 |
| b1 | 0.23 | 0.254 | 0.28 |
| c | 0.20 | ---- | 0.25 |
| c1 | 0.19 | 0.20 | 0.21 |
| D | 4.80 | 4.90 | 5.00 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | ---- | 4.00 |
| e | 0.635BSC | | |
| h | 0.25 | ---- | 0.50 |
| L | 0.50 | 0.65 | 0.80 |
| L1 | 1.05BSC | | |
| θ | 0 | ----- | 8° |

Package Information

SOP16 Package



| SYMBOL | MILLIMETER | | |
|--------|------------|------|-------|
| | MIN | NOM | MAX |
| A | ---- | ---- | 1.75 |
| A1 | 0.05 | ---- | 0.225 |
| A2 | 1.30 | 1.40 | 1.50 |
| A3 | 0.60 | 0.65 | 0.70 |
| b | 0.39 | ---- | 0.48 |
| b1 | 0.38 | 0.41 | 0.43 |
| c | 0.21 | ---- | 0.26 |
| c1 | 0.19 | 0.20 | 0.21 |
| D | 9.70 | 9.90 | 10.10 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.70 | 3.90 | 4.10 |
| e | 1.27BSC | | |
| h | 0.25 | ---- | 0.50 |
| L | 0.50 | ---- | 0.80 |
| L1 | 1.05BSC | | |
| θ | 0 | ---- | 8° |