

## Two Channels Integrated Power Management IC for Handheld Portable Equipment

### Features

- Two Integrated Regulators  
OUT1: 600mA PWM Step-Down DC/DC  
OUT2: Low Noise LDO
- Independent Enable/Disable Control
- Minimal External Components
- 2×2mm, Thin-DFN (TDFN2\*2-8) Package
  - Only 0.75mm Height
  - RoHS Compliant

### Applications

- Portable Devices and PDAs
- MP3/MP4 Players
- Wireless Handhelds
- GPS Receivers, etc.

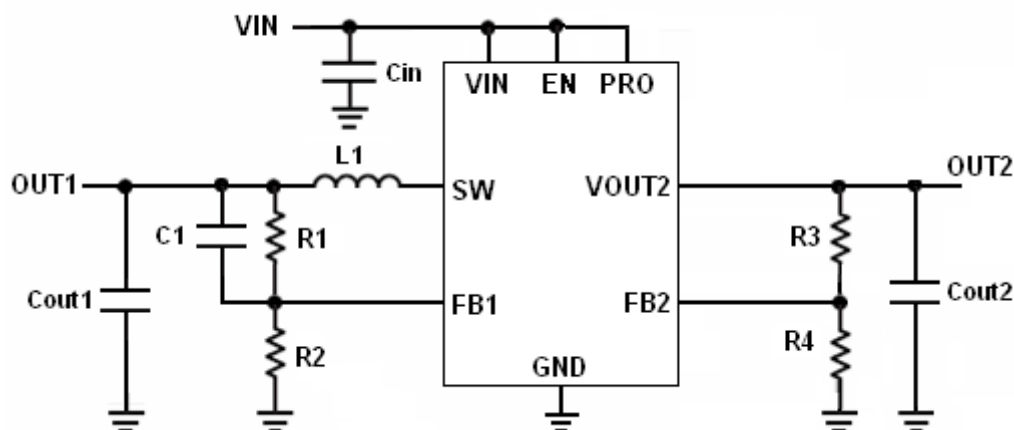
### Description

The HM5062 is a complete, cost effective, highly-efficient power management solution that is ideal for a wide range of portable handheld equipment. This device integrates one PWM step-down DC/DC converter and one low noise, low dropout linear regulators (LDO) in a single, thin, space-saving package. This device is ideal for a wide range of portable handheld equipment that can benefit from the advantages of technology but does not require a high level of integration.

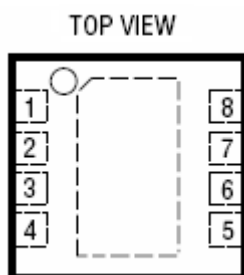
OUT1 is a fixed-frequency, current-mode PWM step-down DC/DC converter that is optimized for high efficiency and is capable of supplying up to 600mA output current. OUT2 are low noise, high PSRR linear regulators that are capable of supplying up to 300mA, and 300mA, respectively.

The HM5062 is available in a tiny 2mm × 2mm 8-pin Thin-DFN package that is just 0.75mm thin.

## Typical Application



## Pin Assignment



DFN2\*2-8

PIN NUMBER DFN2*2-8	PIN NAME	DESCRIPTION
1	SW	Switching node Output for OUT1
2	GND	Power Ground
3	VOUT2	Output voltage for OUT2
4	FB2	Output Feedback Sense for OUT2
5	PRO	Power input for OUT2
6	EN	Enable control input for OUT1, OUT2
7	VIN	Power Input for OUT1
8	FB1	Output Feedback Sense for OUT1

## Absolute Maximum Ratings

- SW to GND, VIN, VPRO, FB1, FB2, VOUT2, EN, to GND..... -0.3~+6V
- SW to VIN..... -6~+0.3V
- Junction to Ambient Thermal Resistance.....33℃/W
- Operating Temperature Range.....-40~85℃
- Junction Temperature.....125℃
- Storage Temperature..... -55~150℃
- Lead Temperature (Soldering, 10 sec)..... 300℃

## Electrical Characteristics (OUT1)

$V_{IN} = 3.6V$ ,  $C_{OUT2} = 1\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Operating Range		2.6		5.5	V
Quiescent Current	$V_{IN}=4.2V$ , $I_{OUT1}=0mA$		260		$\mu A$
Shutdown Current	$V_{IN}=4.2V$ , $EN=0$		0.1		$\mu A$
FB1 Voltage			0.625		V
Load Current Limit			600		mA
Oscillator Frequency	$V_{OUT1} \geq 1.2V$	0.8	1.2	1.5	MHz
	$V_{OUT1} = 0V$		0.53		
PMOS Switch On Resistance	$I_{SW} = -100mA$		0.45	0.75	$\Omega$
NMOS Switch On Resistance	$I_{SW} = 100mA$		0.3	0.45	$\Omega$
SW Leakage Current	$V_{VP1}=5.5V$ , $V_{SW}=5.5V$ or $0V$			1	$\mu A$
Thermal Shutdown Temperature	Temperature Rising		160		$^\circ C$
Thermal Shutdown Hysteresis	Temperature Falling		20		$^\circ C$

## Electrical Characteristics (OUT2)

$V_{PRO} = 3.6V$ ,  $C_{OUT2} = 1\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Operating Range		2		5.5	V
Output Voltage Regulation Accuracy	$T_A = 25^\circ C$	-1.2	$V_{OUT2,3}$	+2	%
	$T_A = -40^\circ C$ to $+85^\circ C$	-2.5	$V_{OUT2,3}$	+3	
Supply Current Per Output	Regulator Enabled		50		$\mu A$
	Regulator Disabled		0		
FB2 Voltage			1.212		V
Output Current Limit			300		mA
Stable $C_{OUT2}$ Range		1		20	$\mu F$
Thermal Shutdown Temperature	Temperature Rising		160		$^\circ C$
Thermal Shutdown Hysteresis	Temperature Falling		20		$^\circ C$

## Pin Description

**SW (PIN1):** Switching node Output for OUT1. Connect this pin to the switching end of the inductor.

**GND (PIN2):** Power Ground. It is as close to the IC as possible.

**VOUT2 (PIN3):** Output voltage for OUT2. It is capable of delivering up to 300mA of output current. Output has high impedance when disabled.

**FB2 (PIN4):** Output Feedback Sense for OUT2. Receives the feedback voltage from an external resistive divider across the output. The output voltage for OUT2 is set by a resistive divider according to the following formula:  $V_{OUT2} = 1.212V \cdot [1 + (R3/R4)]$ .

**PRO (PIN5):** Power input for OUT2. Bypass to GND with a high quality ceramic capacitor placed as close as possible to the IC.

**EN (PIN6):** Enable control input for OUT1, OUT2. Drive EN to the VIN or a logic high for normal operation, drive EN to GND or a logic low to disable OUT1, OUT2.

**VIN (PIN7):** Power Input for OUT1. Bypass to GND with a high quality ceramic capacitor placed as close as possible to the IC.

**FB1 (PIN8):** Output Feedback Sense for OUT1. Receives the feedback voltage from an external resistive divider across the output. The output voltage for OUT1 is set by a resistive divider according to the following formula:  $V_{OUT1} = 0.625V \cdot [1 + (R1/R2)]$ .

## Application Information

The basic HM5062 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by CIN and COUT.

### Inductor Selection

For most applications, the value of the inductor will fall in the range of 1μH to 4.7μH. Its value is chosen based on the desired ripple current. Large value inductors lower ripple current and small value inductors result in higher ripple currents. Higher  $V_{IN}$  or  $V_{OUT}$  also increases the ripple current as shown in equation (1). A reasonable starting point for setting ripple current is  $\Delta I_L = 240\text{mA}$  (40% of 600mA).

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT} \left( 1 - \frac{V_{OUT}}{V_{IN}} \right) \quad (1)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 0.9A rated inductor should be enough for most applications (600mA + 120mA). For better efficiency, choose a low DC-resistance inductor.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or perm alloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs. size requirements and any radiated field/EMI requirements than on what the HM5062 requires to operate. Table 1 shows some typical surface mount inductors that work well in HM5062 applications.

**Table1: Suggested Inductors**

Component Supplier	Series	Inductance (uH)	DCR (mΩ)	Current Rating (mA)	Dimensions (mm)
TAIYO YUDEN	NR 3015	2.2	60	1480	3 x 3 x 1.5
TAIYO YUDEN	NR 3015	4.7	120	1020	3 x 3 x 1.5
Sumida	CDRH2D14	2.2	75	1500	4.5 x 3.2 x 1.55
Sumida	CDRH2D14	4.7	135	1000	4.5 x 3.2 x 1.55
GOTREND	GTSD32	2.2	58	1500	3.85 x 3.85 x 1.8
GOTREND	GTSD32	4.7	146	1100	3.85 x 3.85 x 1.8

## Output and Input Capacitor Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle  $V_{OUT}/V_{IN}$ . To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ required } I_{RMS} \cong I_{OMAX} \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{1/2}}{V_{IN}}$$

This formula has a maximum at  $V_{IN} = 2V_{OUT}$ , where  $I_{RMS} = I_{OUT}/2$ . This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

The selection of  $C_{OUT}$  is driven by the required effective series resistance (ESR). Typically, once the ESR requirement for  $C_{OUT}$  has been met, the RMS current rating generally far exceeds the  $I_{RIPPLE(P-P)}$  requirement. The output ripple  $\Delta V_{OUT}$  is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left( ESR + \frac{1}{8fC_{OUT}} \right)$$

Where  $f$  = operating frequency,  $C_{OUT}$  = output capacitance and  $\Delta I_L$  = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since  $\Delta I_L$  increases with input voltage.

Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum. These are specially constructed and tested for low ESR so they give the lowest ESR for a given volume. Other capacitor types include Sanyo POSCAP, Kemet T510 and T495 series, and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

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## Efficiency Considerations

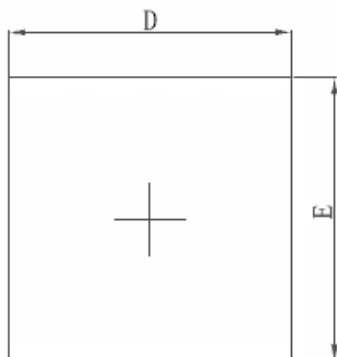
The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:  $\text{Efficiency} = 100\% - (L1 + L2 + L3 + \dots)$  where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: VIN quiescent current and  $I^2R$  losses. The VIN quiescent current loss dominates the efficiency loss at very low load currents whereas the  $I^2R$  loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The VIN quiescent current is due to two components: the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge  $\Delta Q$  moves from VIN to ground. The resulting  $\Delta Q / \Delta t$  is the current out of VIN that is typically larger than the DC bias current. In continuous mode,  $I_{\text{GATECHG}} = f (Q_T + Q_B)$  where  $Q_T$  and  $Q_B$  are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to VIN and thus their effects will be more pronounced at higher supply voltages.

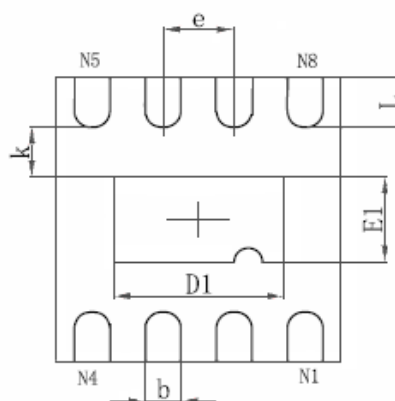
2.  $I^2R$  losses are calculated from the resistances of the internal switches,  $R_{\text{SW}}$  and external inductor  $R_L$ . In continuous mode the average output current flowing through inductor L is “chopped” between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET  $R_{\text{DS(ON)}}$  and the duty cycle (DC) as follows:  $R_{\text{SW}} = R_{\text{DS(ON)TOP}} \times \text{DC} + R_{\text{DS(ON)BOT}} \times (1 - \text{DC})$ . The  $R_{\text{DS(ON)}}$  for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain  $I^2R$  losses, simply add  $R_{\text{SW}}$  to  $R_L$  and multiply the result by the square of the average output current. Other losses including CIN and COUT ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

## Packaging Information

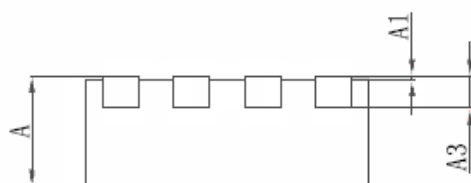
### DFN2\*2-8 Package Outline Dimension



**Top View**



**Bottom View**



**Slide View**

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF		0.008REF	
D	1.900	2.100	0.075	0.083
E	1.900	2.100	0.075	0.083
D1	1.100	1.300	0.043	0.051
E1	0.500	0.700	0.020	0.028
k	0.200MIN		0.008MIN	
b	0.180	0.300	0.007	0.012
e	0.500TYP		0.020TYP	
L	0.250	0.450	0.010	0.018