

N-Channel Super Trench Power MOSFET

Description

The HMS4N10MR uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(on)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

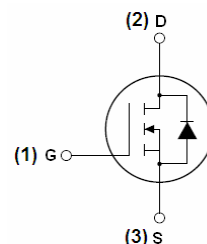
General Features

- $V_{DS} = 100V, I_D = 4A$
 $R_{DS(on)} < 115m\Omega$ (at $V_{GS} = 10V$)
 $R_{DS(on)} < 130m\Omega$ (at $V_{GS} = 4.5V$)
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

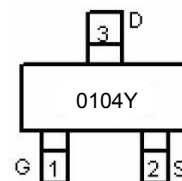
Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

100% UIS TESTED!



Schematic diagram



Marking and pin assignment



SOT-23-3L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
0104Y	HMS4N10MR	SOT23-3L	Ø330mm	12mm	2500 units

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	4	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	2.8	A
Pulsed Drain Current	I_{DM}	12	A
Maximum Power Dissipation	P_D	3.5	W
Derating factor		0.028	W/ $^\circ C$
Single pulse avalanche energy (Note 5)	E_{AS}	196	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	36	$^{\circ}\text{C/W}$
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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

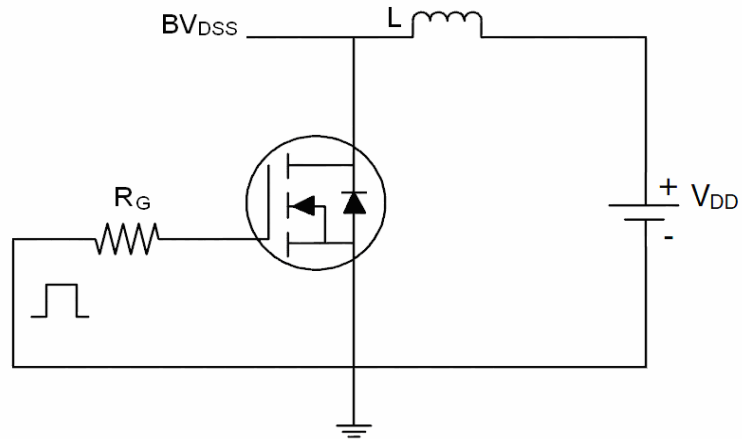
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	0.8	1.2	1.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =4A	-	95	115	mΩ
		V _{GS} =4.5V, I _D =4A	-	115	130	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =4A	-	45	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, F=1.0MHz	3600	4200	5480	PF
Output Capacitance	C _{oss}		-	354	425	PF
Reverse Transfer Capacitance	C _{rss}		-	23	30	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =50V, I _D =4A V _{GS} =10V, R _G =1.6Ω	-	14	-	nS
Turn-on Rise Time	t _r		-	9	-	nS
Turn-Off Delay Time	t _{d(off)}		-	39	-	nS
Turn-Off Fall Time	t _f		-	5	-	nS
Total Gate Charge	Q _g	V _{DS} =50V, I _D =4A, V _{GS} =10V	-	58	-	nC
Gate-Source Charge	Q _{gs}		-	12	-	nC
Gate-Drain Charge	Q _{gd}		-	7.8	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V, I _S =4A	-	-	1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	8	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = I _S	-	101	-	nS
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs ^(Note3)	-	193	-	nC

Notes:

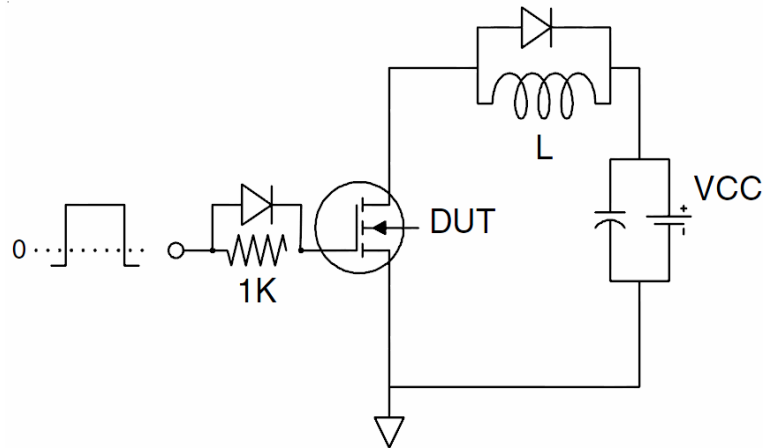
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5\text{mH}, R_g=25\Omega$

Test Circuit

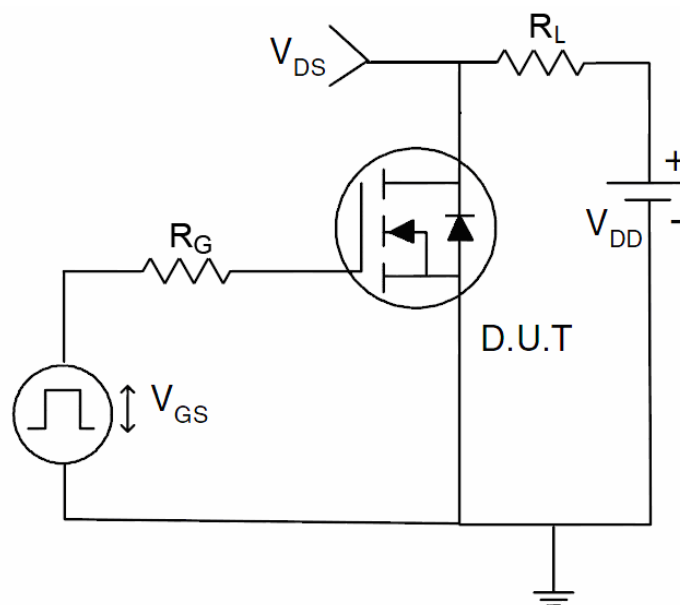
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

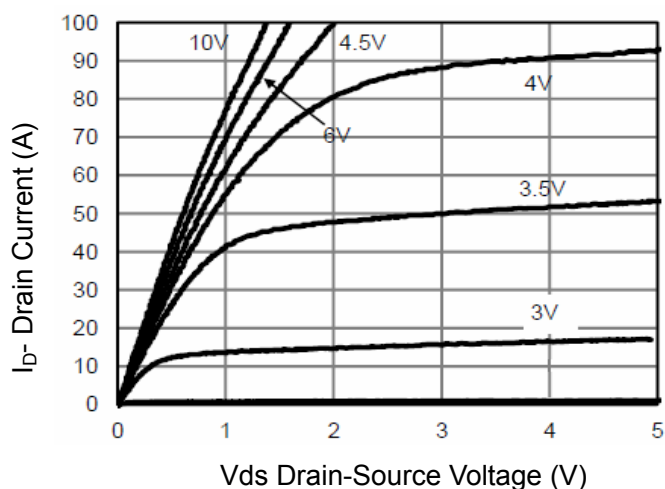


Figure 1 Output Characteristics

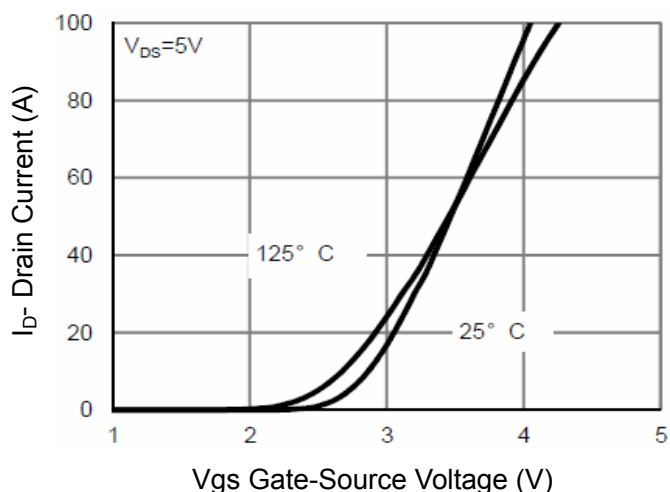


Figure 2 Transfer Characteristics

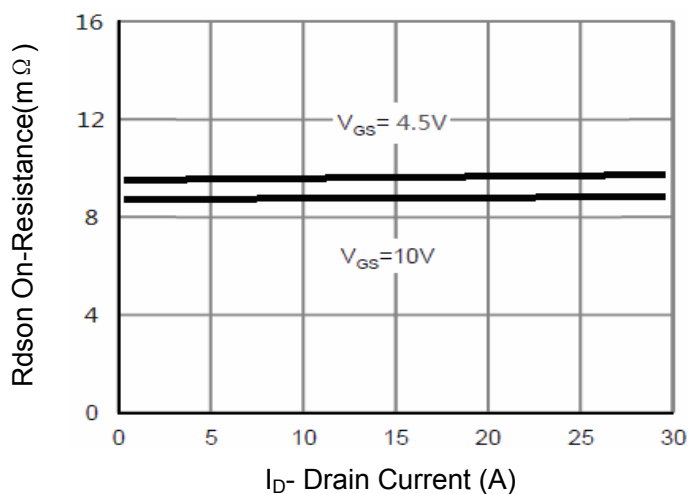


Figure 3 Rdson- Drain Current

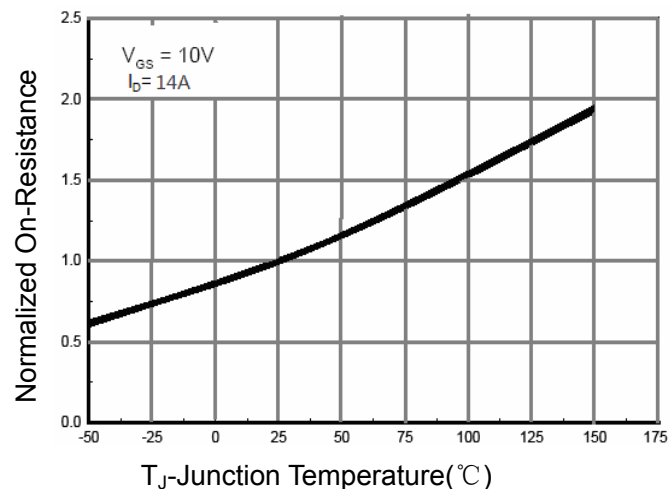


Figure 4 Rdson-Junction Temperature

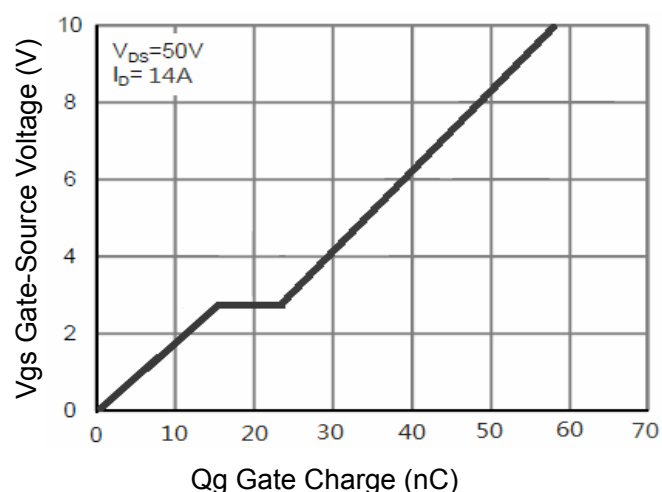


Figure 5 Gate Charge

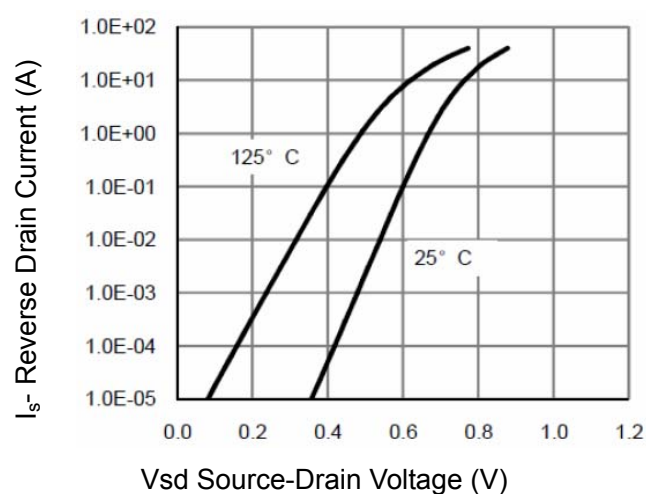


Figure 6 Source- Drain Diode Forward

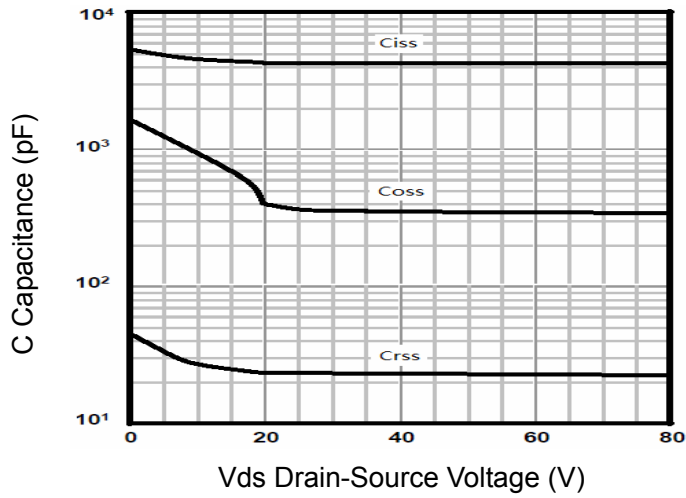


Figure 7 Capacitance vs Vds

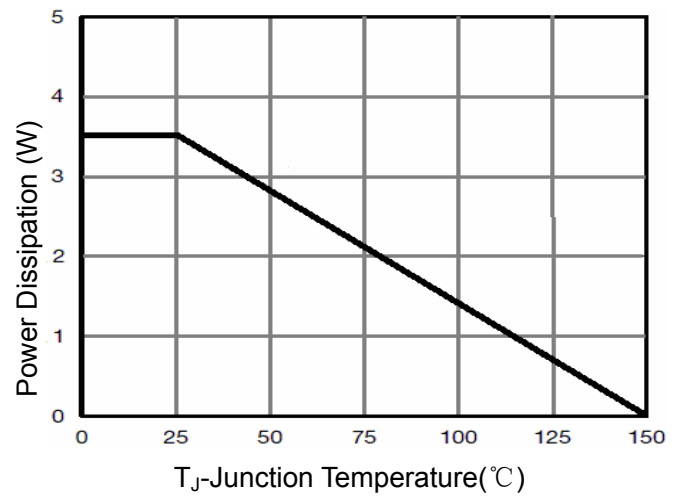


Figure 9 Power De-rating

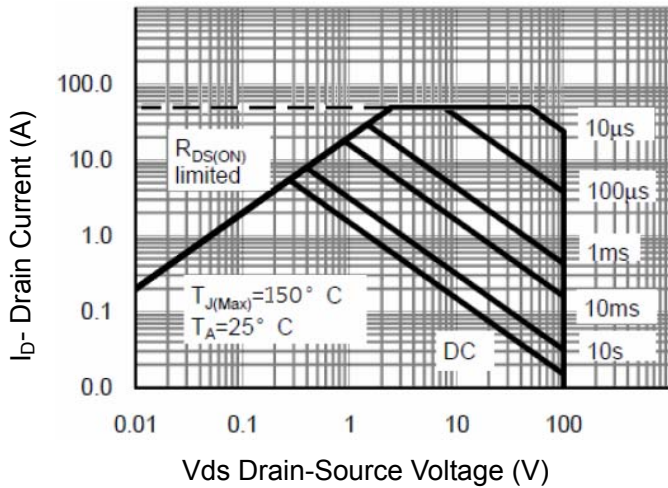


Figure 8 Safe Operation Area

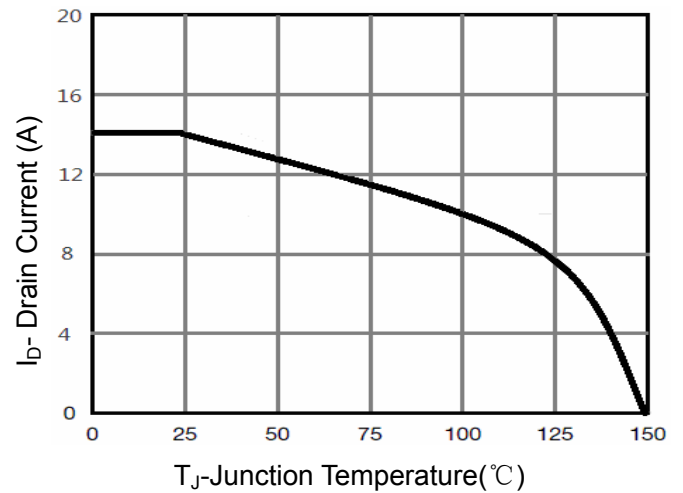


Figure 10 Current De-rating

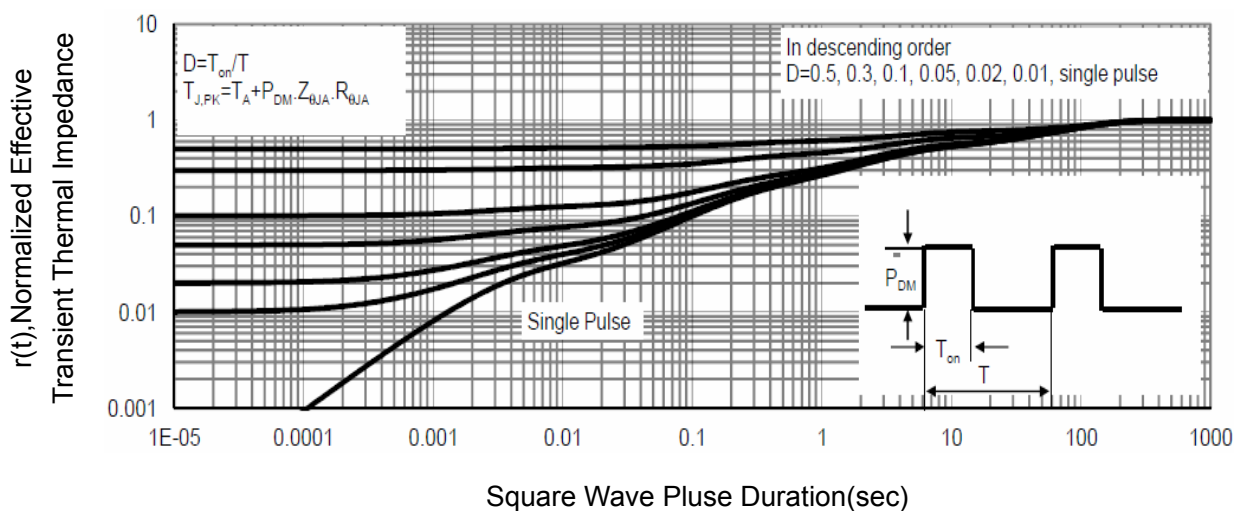
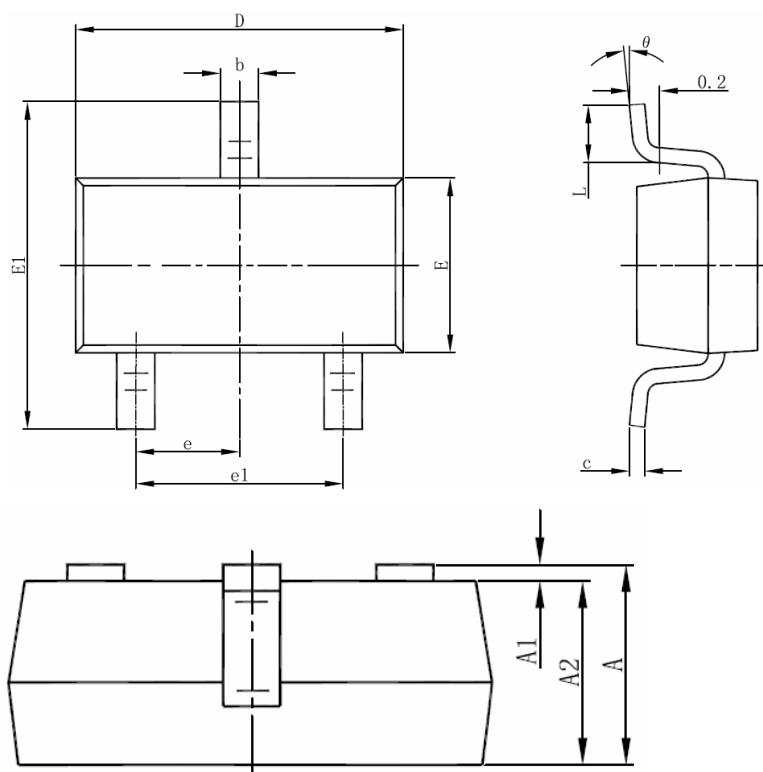


Figure 11 Normalized Maximum Transient Thermal Impedance

SOT-23-3L PACKAGE INFORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

NOTES

1. All dimensions are in millimeters.
2. Tolerance $\pm 0.10\text{mm}$ (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

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