

650V GaN Power Transistor (FET)

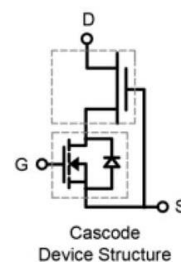
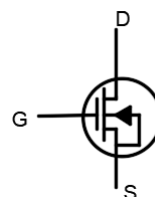
Features

- Easy to use, compatible with standard gate drivers
- Superior reliability with BV_{DSS} over 1500V
- Excellent $Q_g \times R_{DS(on)}$ figure of merit (FOM)
- Low Q_{rr} , no free-wheeling diode required
- Low switching loss
- RoHS compliant and Halogen-free

Product Summary		
V_{DSS}	650	V
$R_{DS(on), typ}$	230	mΩ
$Q_{G, typ}$	12.5	nC
$Q_{RR, typ}$	38	nC

Applications

- High efficiency power supplies
- High efficiency USB PD adapters
- Other consumer electronics



Packaging

Part Number	Package	Packaging	Base QTY
HMN11N65D	DFN 8 x 8	Tape and Reel	2500

Maximum ratings, at $T_C=25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter		Limit Value	Unit
I_D	Continuous drain current @ $T_C=25^\circ\text{C}$		11	A
	Continuous drain current @ $T_C=100^\circ\text{C}$		7	A
I_{DM}	Pulsed drain current @ $T_C=25^\circ\text{C}$ (pulse width: 10us)		39	A
	Pulsed drain current @ $T_C=150^\circ\text{C}$ (pulse width: 10us)		30	A
V_{DSS}	Drain to source voltage ($T_J = -55^\circ\text{C}$ to 150°C)		650	V
V_{GSS}	Gate to source voltage		± 20	V
P_D	Maximum power dissipation @ $T_C=25^\circ\text{C}$		50	W
T_C	Operating temperature	Case	-55 to 150	$^\circ\text{C}$
T_J		Junction	-55 to 150	$^\circ\text{C}$
T_S	Storage temperature		-55 to 150	$^\circ\text{C}$
T_{CSOLD}	Soldering peak temperature		260	$^\circ\text{C}$

Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Junction-to-case	2.5	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient ^a	50	$^{\circ}\text{C}/\text{W}$

Notes:

- a. Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6cm² copper area and 70μm thickness)

Electrical Parameters, at $T_J=25\text{ }^{\circ}\text{C}$, unless otherwise specified

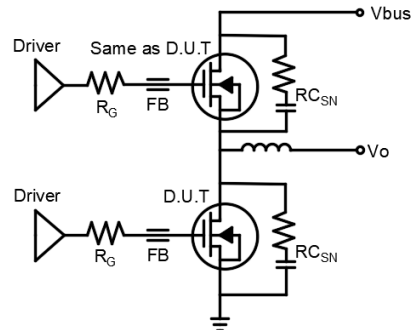
Symbol	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics					
V _{DSS-MAX}	650	-	-	V	V _{GS} =0V
BV _{DSS}	-	1500	-	V	V _{GS} =0V, I _{DSS} =250μA
V _{GS(th)}	1.5	1.8	2.1	V	V _{DS} =V _{GS} , I _D =500μA
R _{DS(on)} ^a	-	230	270	mΩ	V _{GS} =8V, I _D =4A, T _J =25°C
	-	450	-		V _{GS} =8V, I _D =4A, T _J =150°C
I _{DSS}	-	8	20	μA	V _{DS} =700V, V _{GS} =0V, T _J =25°C
	-	25	-	μA	V _{DS} =700V, V _{GS} =0V, T _J =150°C
I _{GSS}	-	-	150	nA	V _{GS} =20V
	-	-	-150	nA	V _{GS} =-20V
C _{ISS}	-	490	-	pF	V _{GS} =0V, V _{DS} =650V, f=1MHz
C _{OSS}	-	25	-	pF	
C _{RSS}	-	4	-	pF	
C _{O(er)}	-	30	-	pF	V _{GS} =0V, V _{DS} =0 - 650V
C _{O(tr)}	-	50	-	pF	
Q _G	-	12.5	-	nC	V _{DS} =400V, V _{GS} =0 - 8V, I _D =10A
Q _{GS}	-	3	-		
Q _{GD}	-	2.8	-		
t _{D(on)}	-	16	-	nS	V _{DS} =400V, V _{GS} =0 - 12V, I _D =10A, R _G =33 Ω
t _R	-	13	-		
t _{D(off)}	-	80	-		
t _F	-	7	-		
Reverse Device Characteristics					
V _{SD}	-	1.7	-	V	V _{GS} =0V, I _S =5A, T _J =25°C
	-	2.6	-		V _{GS} =0V, I _S =10A, T _J =25°C
	-	5	-		V _{GS} =0V, I _S =10A, T _J =150°C
t _{RR}	-	18	-	ns	I _S =10A, V _{GS} =0V, d _i /d _t =1200A/us, V _{DD} =400V
Q _{RR}	-	38	-	nC	

Notes:

a. Dynamic on-resistance; see Figure 18

Circuit Implementation

(1) Mostly used in half bridge and full bridge topology



Recommended Half-bridge Drive Circuit

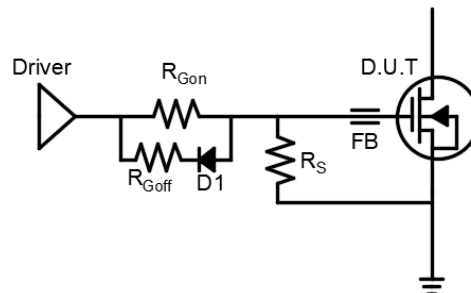
Recommended gate drive: (0 V, 12 V) with $R_G = 33 \Omega$

Gate Ferrite Bead (FB)	Gate Resistance (R_G)	RC Snubber (R_{Csn})
300 Ω @100MHz	33 Ω	22 pF + 15 Ω

Notes:

- R_{Csn} should be placed as close as possible to the drain pin
- The layout and wiring of the drive circuit should be as short as possible

(2) Mostly used in flyback, forward and push-pull converters



Recommended Single Ended Drive Circuit

Recommended gate drive: (0 V, 12 V) with $R_{Gon} = 300 - 500 \Omega$, $R_{Goff} = 20 - 50 \Omega$

Gate Ferrite Bead (FB)	Gate Resistance (R_{Gon})	Gate Resistance (R_{Goff})	Gate Source Resistance (R_S)	Gate Diode (D1)
300 - 600 Ω @100MHz	300 - 500 Ω	20 - 50 Ω	10 k Ω	1N4148

Typical Characteristics, at $T_C=25^\circ\text{C}$, unless otherwise specified

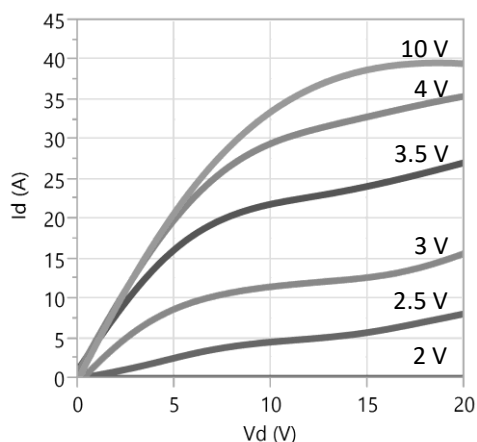


Figure 1. Typical Output Characteristics $T_j=25^\circ\text{C}$

Parameter: V_{GS}

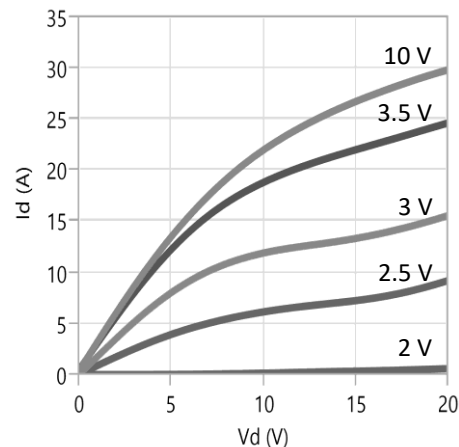


Figure 2. Typical Output Characteristics $T_j=150^\circ\text{C}$

Parameter: V_{GS}

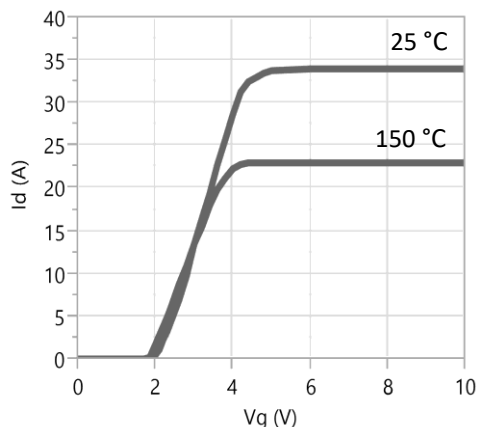


Figure 3. Typical Transfer Characteristics

$V_{DS}=10\text{V}$, Parameter: T_j

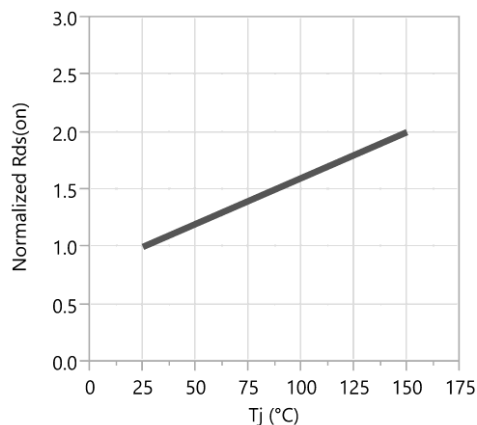


Figure 4. Normalized On-resistance

$I_D=4\text{A}$, $V_{GS}=8\text{V}$

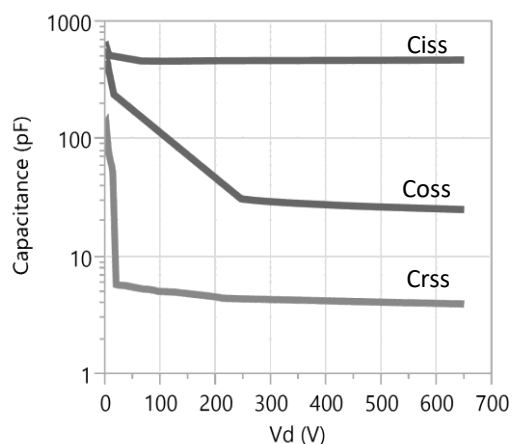


Figure 5. Typical Capacitance

$V_{GS}=0\text{V}$, $f=1\text{MHz}$

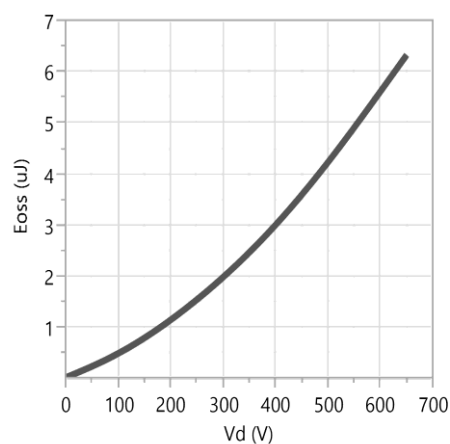


Figure 6. Typical C_{oss} Stored Energy

Typical Characteristics, at $T_C=25^\circ\text{C}$, unless otherwise specified

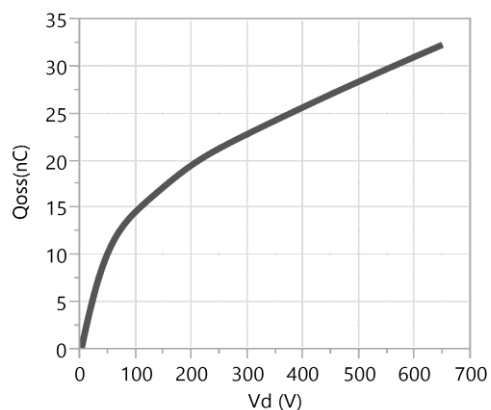


Figure 7. Typical Qoss

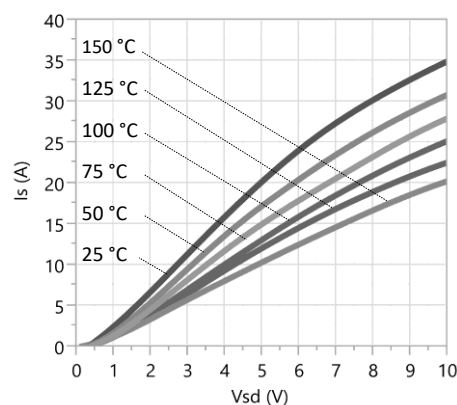


Figure 8. Forward Characteristic of Rev. Diode

$I_s=f(V_s)$, Parameter T_j

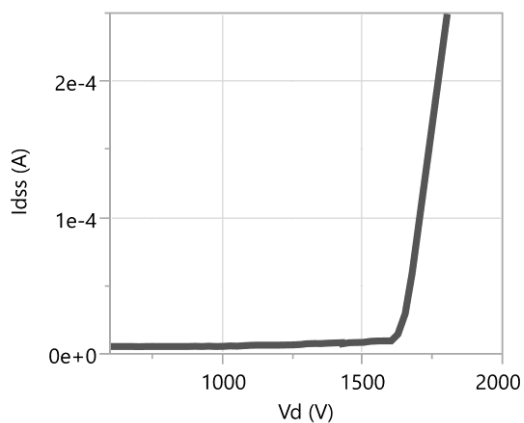


Figure 9. Drain-Source Breakdown Voltage

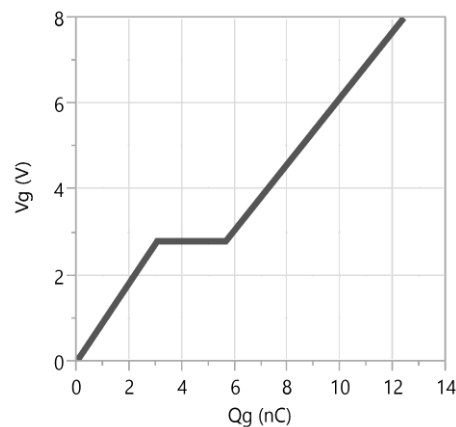


Figure 10. Typical Gate Charge

$I_{DS}=10A$, $V_{DS}=400V$

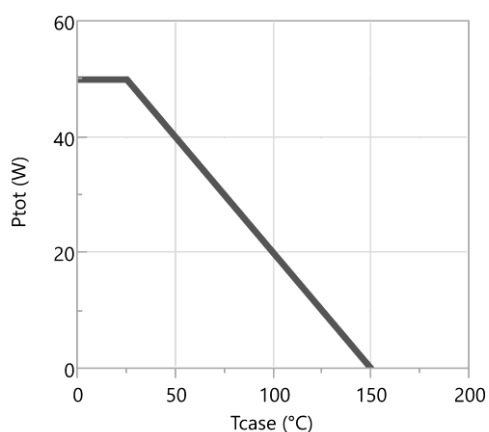


Figure 11. Power Dissipation

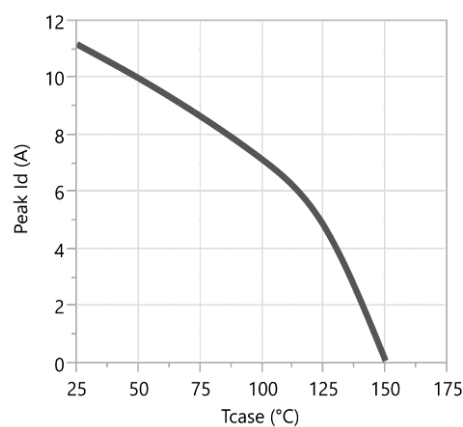


Figure 12. Current Derating

Typical Characteristics, at $T_C=25^\circ\text{C}$, unless otherwise specified

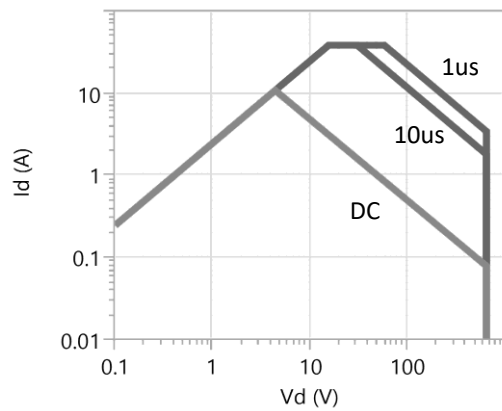


Figure 13. Safe Operating Area $T_C=25^\circ\text{C}$

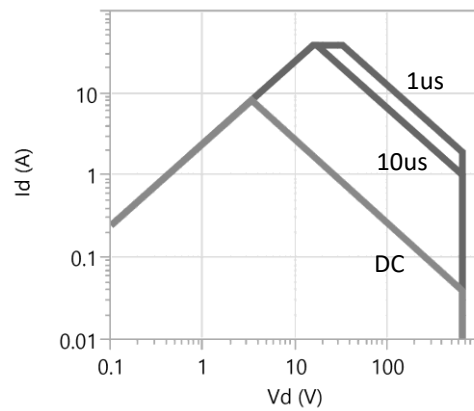


Figure 14. Safe Operating Area $T_C=80^\circ\text{C}$

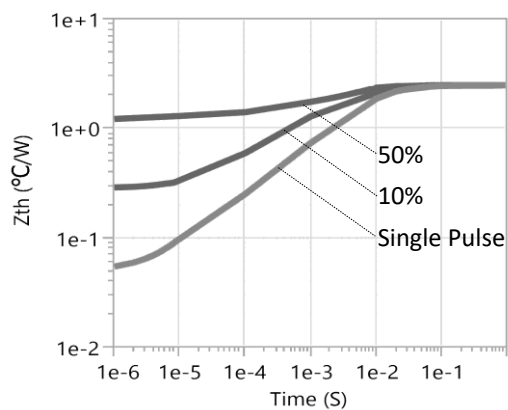


Figure 15. Transient Thermal Resistance

Test Circuits and Waveforms

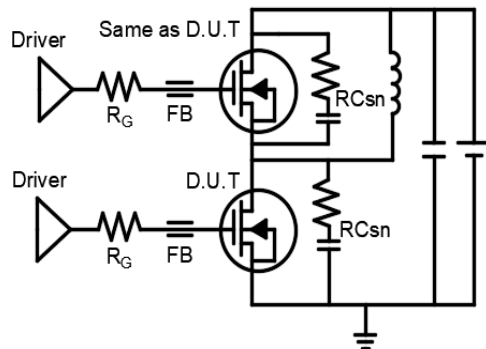


Figure 16. Switching Time Test Circuit

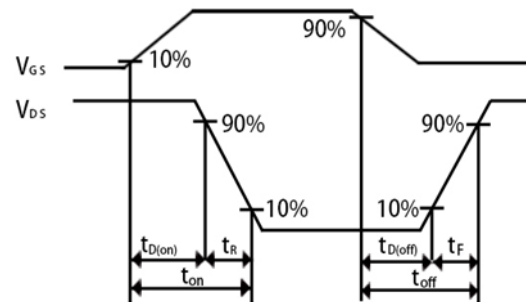


Figure 17. Switching Time Waveform

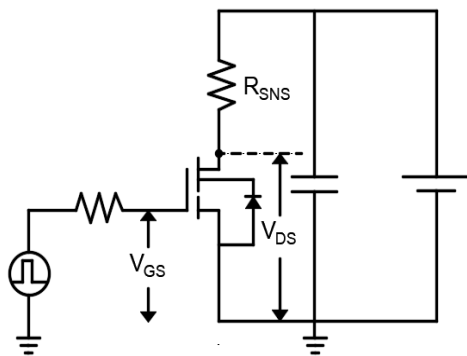


Figure 18. Dynamic $R_{DS(on)}$ Test Circuit

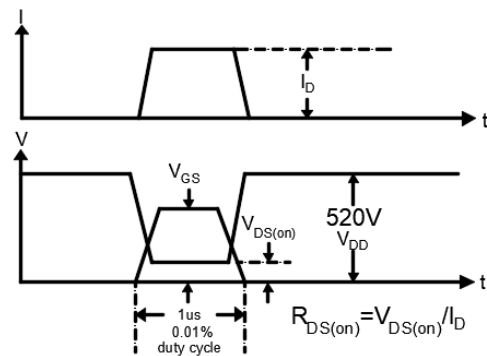


Figure 19. Dynamic $R_{DS(on)}$ Waveform

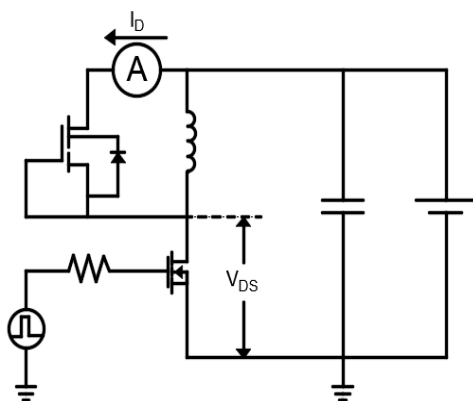


Figure 20. Diode Characteristic Test Circuits

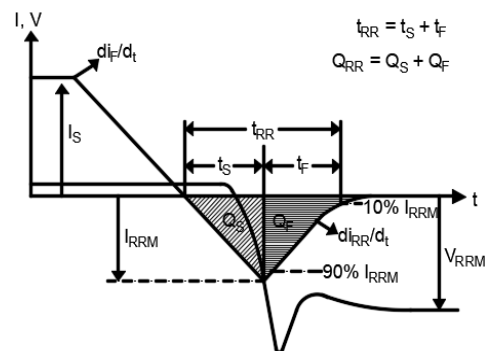


Figure 21. Diode Recovery Waveform

Design Guidelines

Fast switching GaN device can reduce power conversion losses, and thus enable high frequency operations. Certain PCB design rules and instructions, however, need to be followed to take full advantages of fast switching GaN devices.

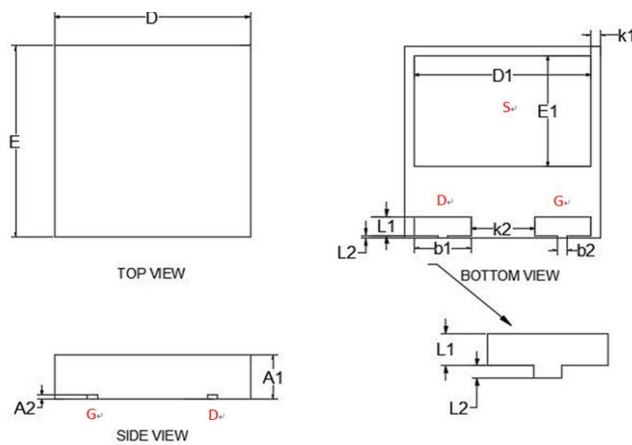
Before evaluating H&M Semi's GaN devices, please refer to the table below which provides some practical rules that should be followed during the evaluation.

When Evaluating = Using H&M Semi's GaN Devices:

DO	DO NOT
Make sure the traces are as short as possible for both drive and power loops to minimize parasitic inductance	Using H&M Semi's devices in GDS board layouts
Use the test tool with the shortest inductive loop, and make sure test points should be placed close enough	Use differential mode probe or probe ground clip with long wires
Minimize the lead length of TO packages when installing them to PCB	Use long traces in drive circuit, or long lead length of the devices

Package Outline

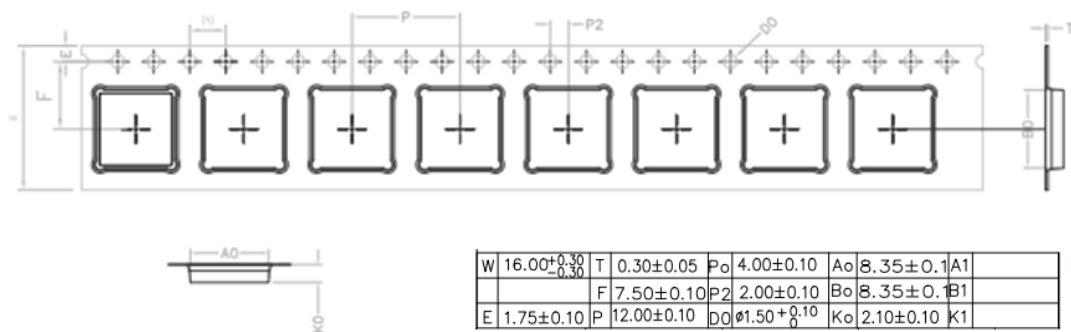
DFN 8 x 8mm (HS) Package



Symbol	Dimensions in Millimeters		
	MIN	NOM	MAX
A1	1.750	1.850	1.950
A2	0.185	0.203	0.230
D	7.000	8.000	9.000
E	7.950	8.000	8.050
D1	7.050	7.200	7.350
E1	4.450	4.600	4.750
K1	0.375	0.400	0.425
K2	2.575	2.600	2.625
b1	2.250	2.300	2.350
b2	0.375	0.400	0.425
L1	0.700	0.800	0.900
L2	0.075	0.100	0.125

Tape and Reel Information

Dimensions are shown in millimeters



Recommended PCB Layout

Dimensions are shown in millimeters

