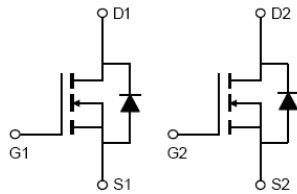


## P-Channel Enhancement Mode Field Effect Transistor



### Product Summary

- $V_{DS}$  -60V
- $I_D$  -10A
- $R_{DS(ON)}$  (at  $V_{GS} = -4.5V$ ) <135mohm
- $R_{DS(ON)}$  (at  $V_{GS} = -10V$ ) <85mohm

### General Description

- Trench Power MV MOSFET technology
- High density cell design for Low  $R_{DS(ON)}$
- High Speed switching

### Applications

- Battery protection
- Load switch
- Power management

### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		$V_{DS}$	-60	V
Gate-source Voltage		$V_{GS}$	$\pm 10$	V
Drain Current <sup>B</sup>	$T_A=25^\circ\text{C}$ @ Steady State	$I_D$	-10	A
	$T_A=100^\circ\text{C}$ @ Steady State		-7	
Drain Current <sup>B</sup>	$T_A=25^\circ\text{C}$ @ Steady State	$I_D$	-10	A
	$T_A=70^\circ\text{C}$ @ Steady State		-7	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	-55	A
Single Pulse Avalanche Energy <sup>B</sup>		$E_{AS}$	31	mJ
Total Power Dissipation <sup>B</sup>	$T_A=25^\circ\text{C}$ @ Steady State	$P_D$	32	W
	$T_A=100^\circ\text{C}$ @ Steady State		12.8	
Total Power Dissipation <sup>B</sup>	$T_A=25^\circ\text{C}$ @ Steady State	$P_D$	3	W
	$T_A=70^\circ\text{C}$ @ Steady State		1.9	
Thermal Resistance Junction-to-Ambient @ Steady State <sup>B</sup>		$R_{\theta JC}$	3.9	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-to-Case @ Steady State <sup>C</sup>		$R_{\theta JA}$	42	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	$^\circ\text{C}$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
HM10DP06D	F1	HM10DP06D XXXX	5000	10000	100000	13" reel

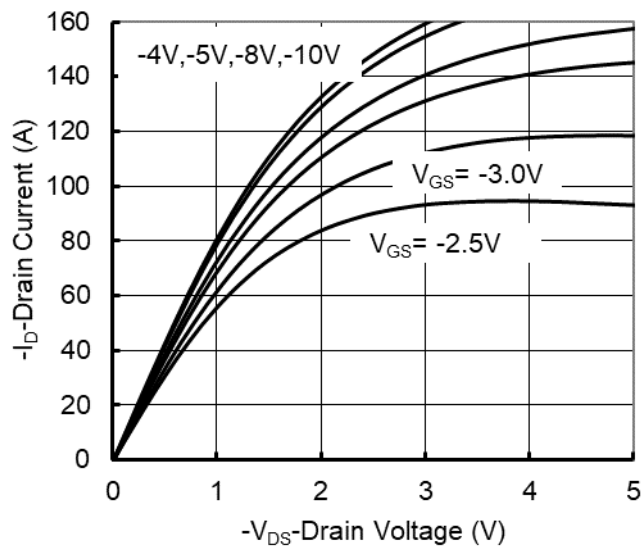
■ Electrical Characteristics (T<sub>J</sub>=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-60V,V <sub>GS</sub> =0V,T <sub>C</sub> =25℃			-1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±10V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.0		-3.0	V
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = -4.5V, I <sub>D</sub> =-5A			135	mΩ
		V <sub>GS</sub> = -10V, I <sub>D</sub> =-1A			85	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-60A,V <sub>GS</sub> =0V		-0.8	-1.2	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				-10	A
Dynamic Parameters						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-10V,V <sub>GS</sub> =0V,f=1MHZ		2992		pF
Output Capacitance	C <sub>oss</sub>			330		
Reverse Transfer Capacitance	C <sub>rss</sub>			272		
Switching Parameters						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =-10V,V <sub>DS</sub> =-15V,I <sub>D</sub> =-9.1A		72.8		nC
Gate Source Charge	Q <sub>gs</sub>			6.6		
Gate Drain Charge	Q <sub>gd</sub>			10.1		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =-6A, di/dt=100A/us		34		ns
Reverse Recovery Time	t <sub>rr</sub>			67		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =-10V,V <sub>DS</sub> =-15V, I <sub>D</sub> =-6A, R <sub>GEN</sub> =2.5Ω		7		
Turn-on Rise Time	t <sub>r</sub>			33		
Turn-off Delay Time	t <sub>D(off)</sub>			130		
Turn-off Fall Time	t <sub>f</sub>			132		

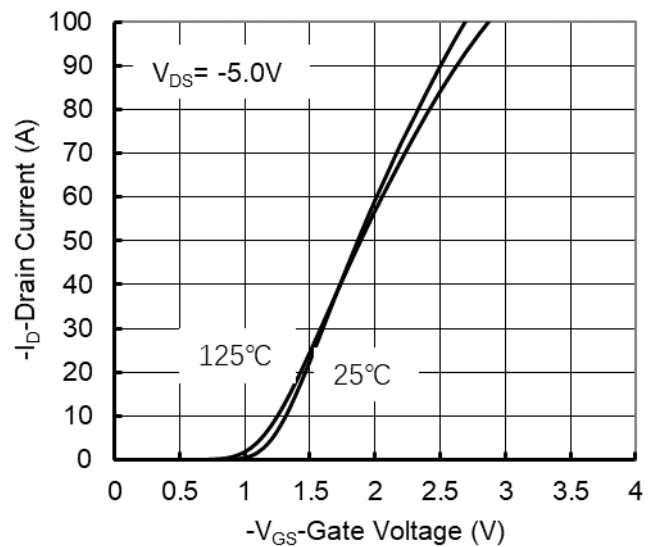
A. Pulse Test: Pulse Width≤300us, Duty cycle ≤2%.

B. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design, while R<sub>θJA</sub> is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

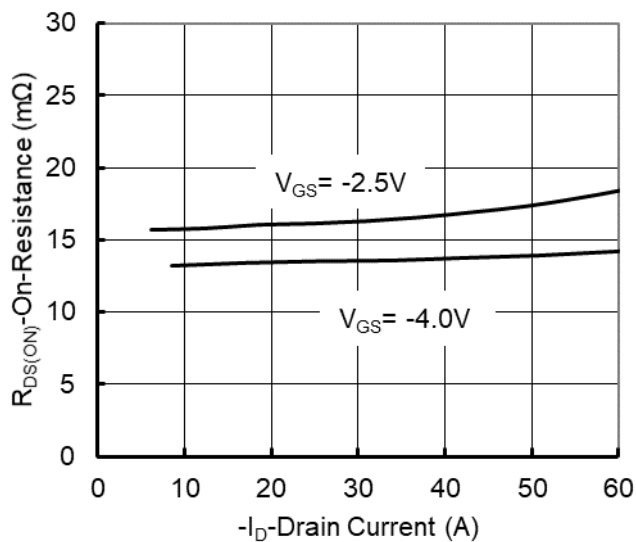
## ■ Typical Performance Characteristics



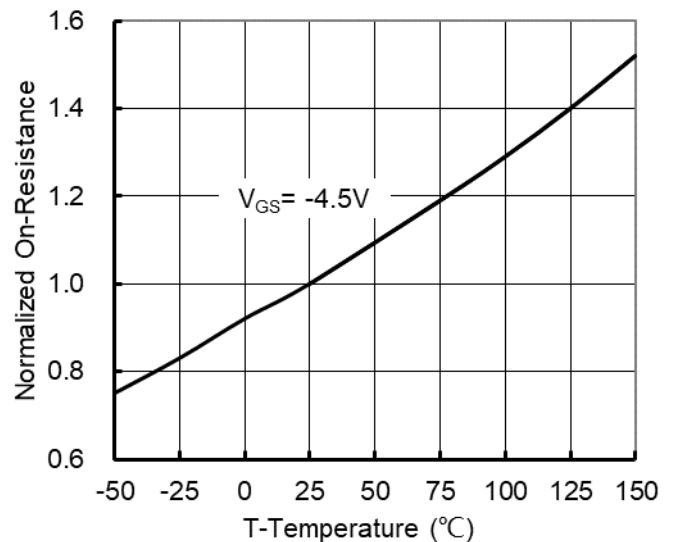
**Figure 1. Output Characteristics**



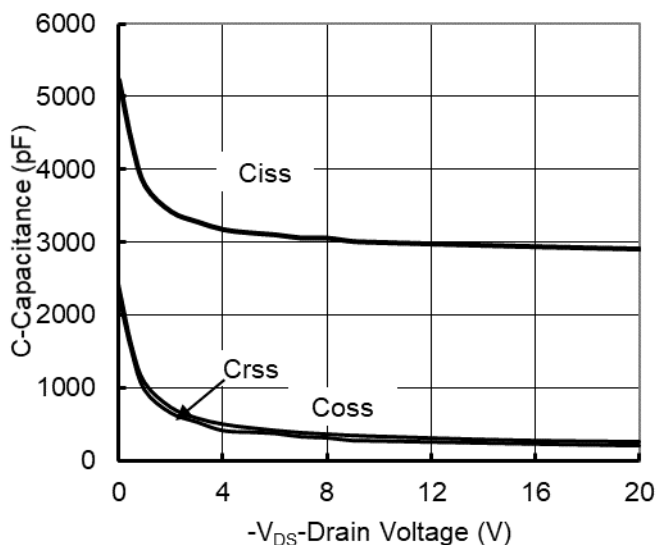
**Figure 2. Transfer Characteristics**



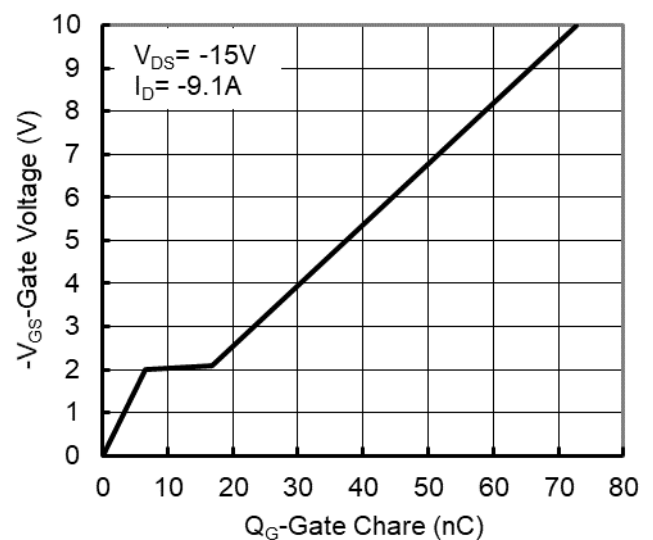
**Figure 3. On-Resistance vs. Drain Current and Gate Voltage**



**Figure 4. On-Resistance vs. Junction Temperature**



**Figure 5. Capacitance Characteristics**



**Figure 6. Gate Charge**

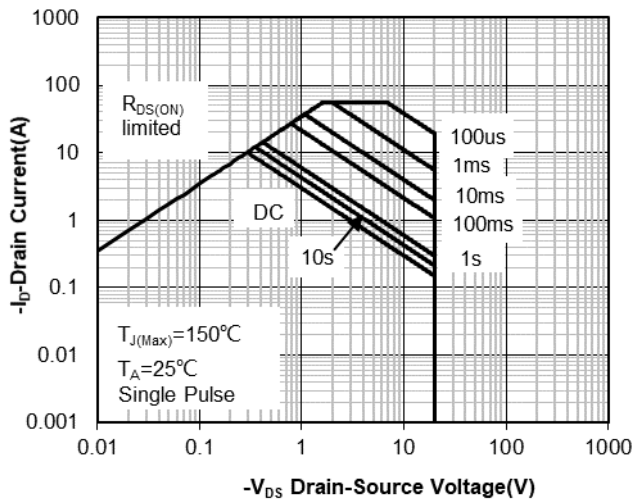


Figure 7. Safe Operation Area

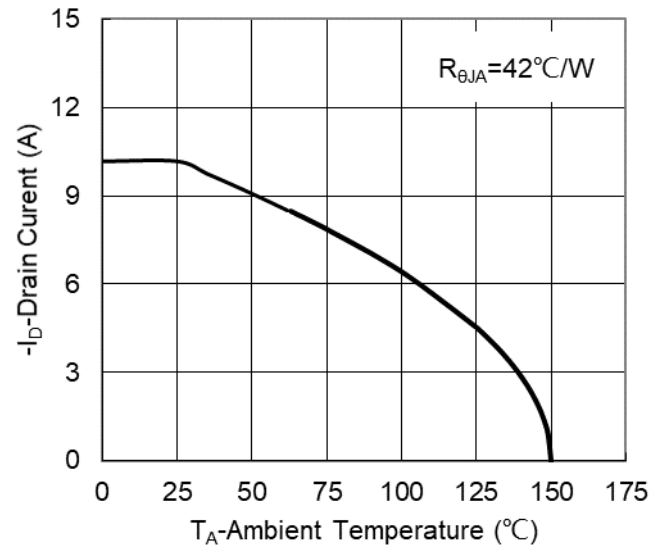


Figure 8. Maximum Continuous Drain Current vs Ambient Temperature

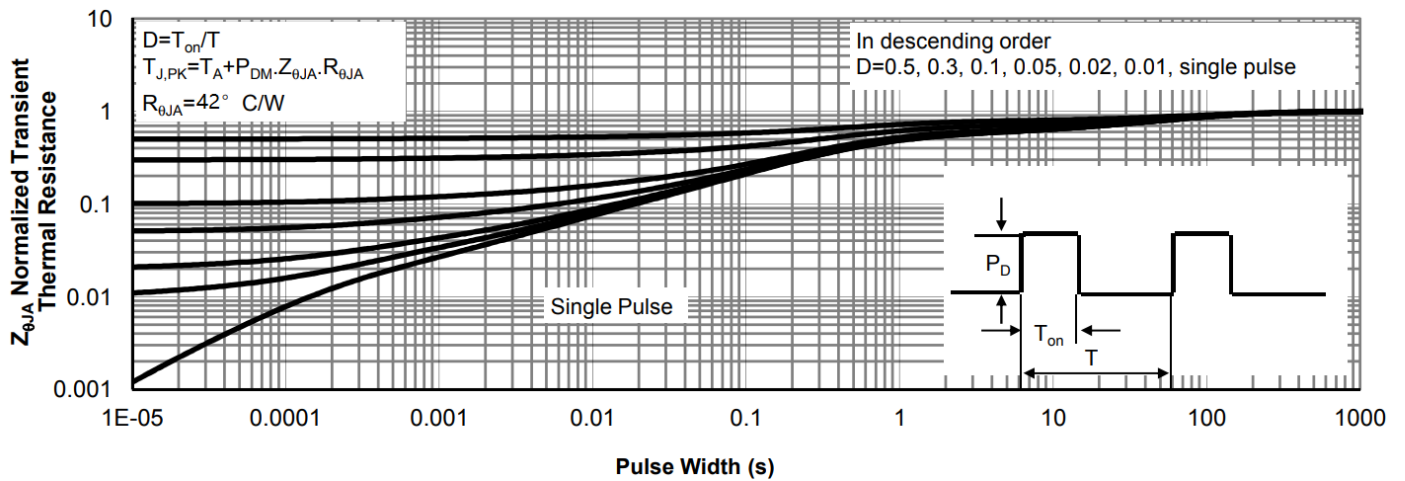
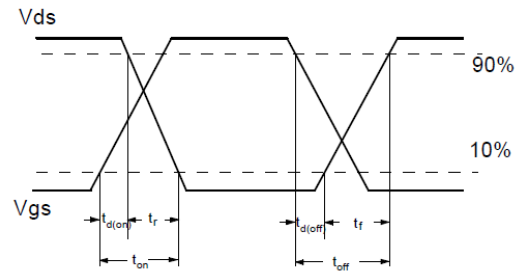
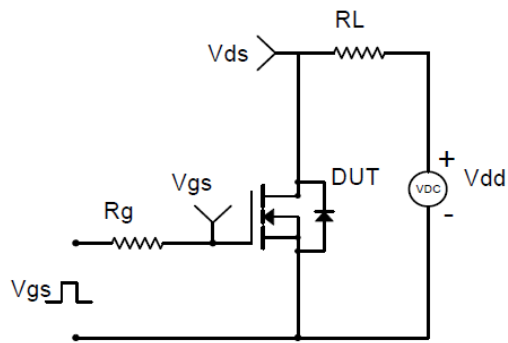
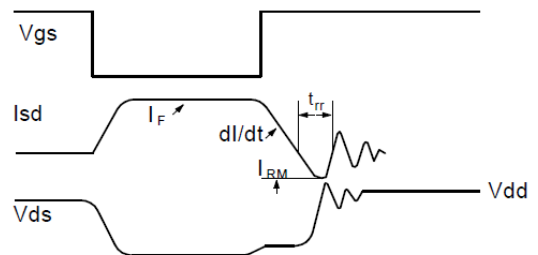
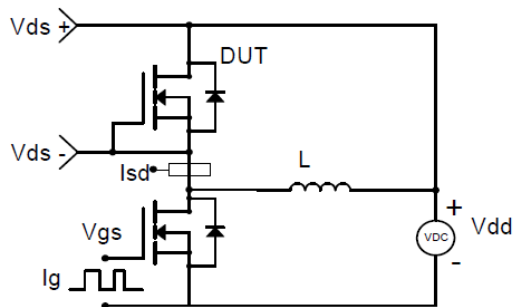


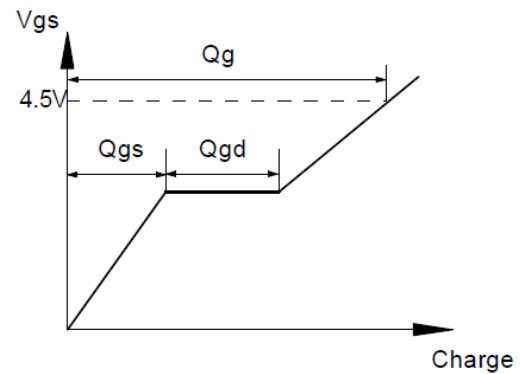
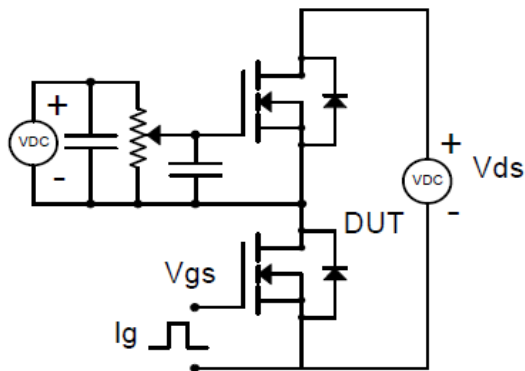
Figure 9. Normalized Maximum Transient Thermal Impedance



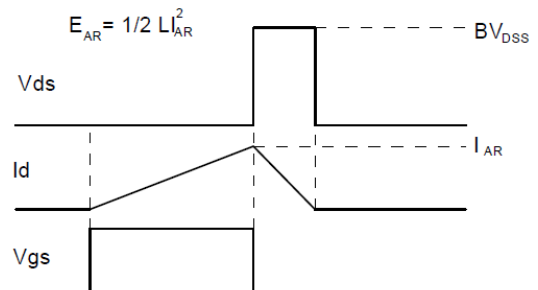
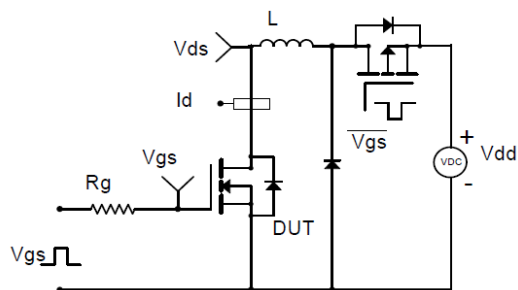
**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**

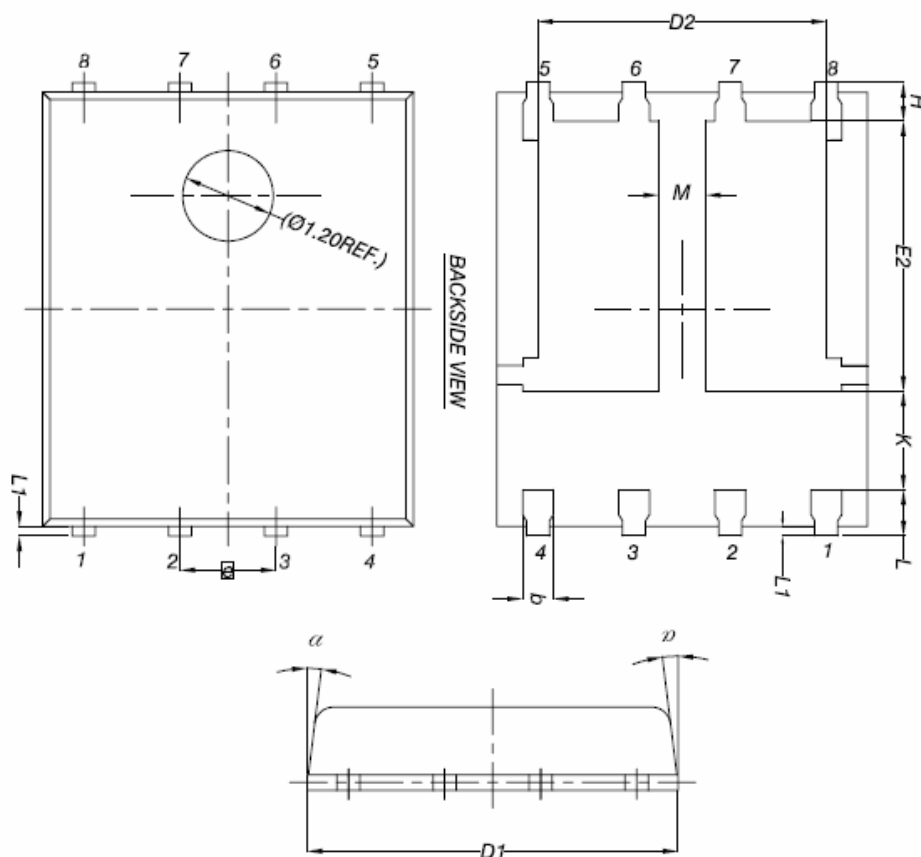


**Gate Charge Test Circuit & Waveform**



**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**

# DFN5X6-8L Package Information



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
M	0.50	-	-
$\alpha$	0°	-	12°

