

N-Channel Enhancement Mode Power MOSFET

Description

The HM4490B uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

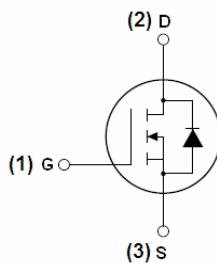
General Features

- $V_{DS} = 200V, I_D = 2A$
- $R_{DS(ON)} < 79m\Omega @ V_{GS}=10V$ (Typ: $580m\Omega$)
- High density cell design for ultra low $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Low gate to drain charge to reduce switching losses

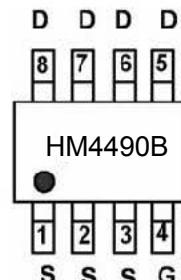
Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

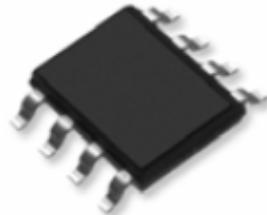
100% ΔV_{ds} TESTED!



Schematic diagram



Marking and pin assignment



SOP-8 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM4490B	HM4490B	SOP-8	Ø330mm	12mm	2500 units

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	200	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	2	A
Drain Current-Continuous($T_C=100^\circ C$)	$I_D (100^\circ C)$	1.4	A
Pulsed Drain Current	I_{DM}	6	A
Maximum Power Dissipation	P_D	3	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	R_{eJC}	41.7	°C/W
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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

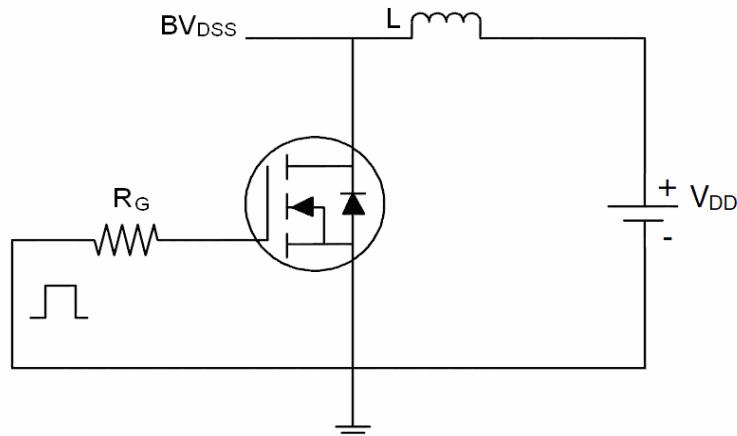
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	200	215	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=200\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	0.7	1.5	2.3	V
Drain-Source On-State Resistance	$R_{\text{DS(ON)}}$	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=3.7\text{A}$	-	440	580	$\text{m}\Omega$
Forward Transconductance	g_{FS}	$V_{\text{DS}}=50\text{V}, I_{\text{D}}=2.0\text{A}$	7	-	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{\text{DS}}=25\text{V}, V_{\text{GS}}=0\text{V}, F=1.0\text{MHz}$		4200		PF
Output Capacitance	C_{oss}			163		PF
Reverse Transfer Capacitance	C_{rss}			75		PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{\text{d(on)}}$	$V_{\text{DD}}=100\text{V}, I_{\text{D}}=2.2\text{A}$ $V_{\text{GS}}=10\text{V}, R_{\text{GEN}}=6.5\Omega$	-	15	-	nS
Turn-on Rise Time	t_r		-	13	-	nS
Turn-Off Delay Time	$t_{\text{d(off)}}$		-	26	-	nS
Turn-Off Fall Time	t_f		-	14	-	nS
Total Gate Charge	Q_g	$V_{\text{DS}}=100\text{V}, I_{\text{D}}=2.2\text{A}, V_{\text{GS}}=10\text{V}$	-	38	-	nC
Gate-Source Charge	Q_{gs}		-	9	-	nC
Gate-Drain Charge	Q_{gd}		-	15	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{\text{GS}}=0\text{V}, I_{\text{S}}=3.7\text{A}$	-	-	1.2	V
Diode Forward Current ^(Note 2)	I_{S}		-	-	4	A

Notes:

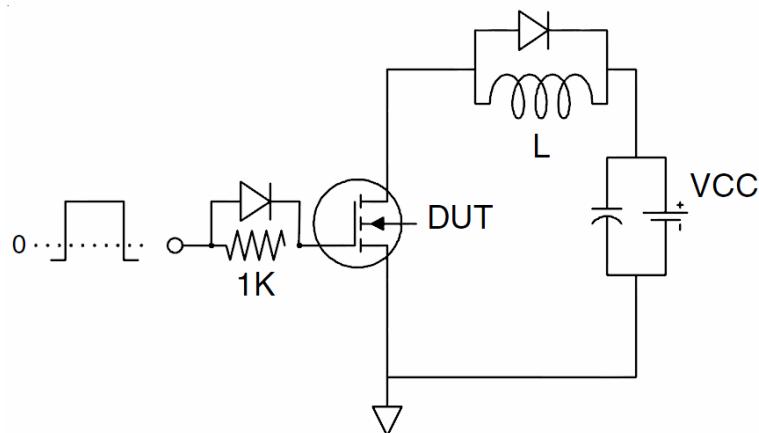
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

Test Circuit

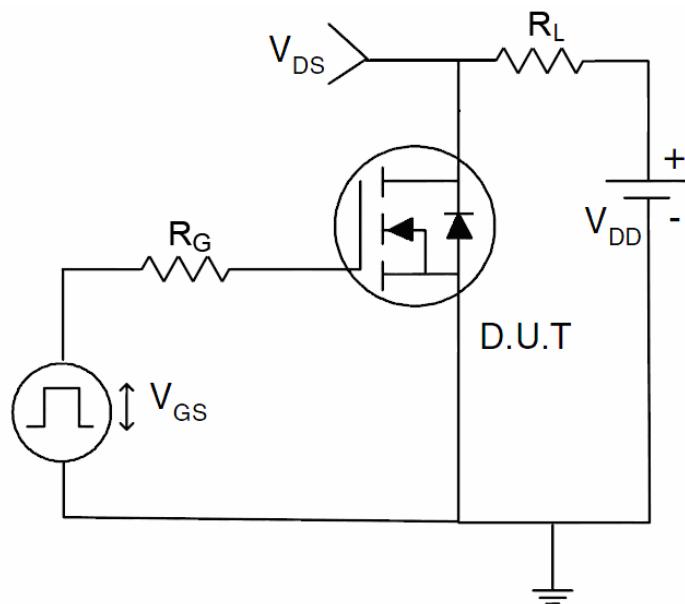
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

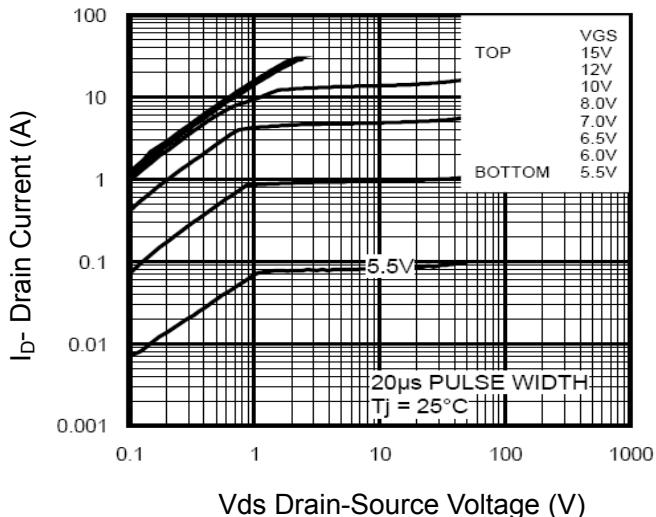


Figure 1 Output Characteristics

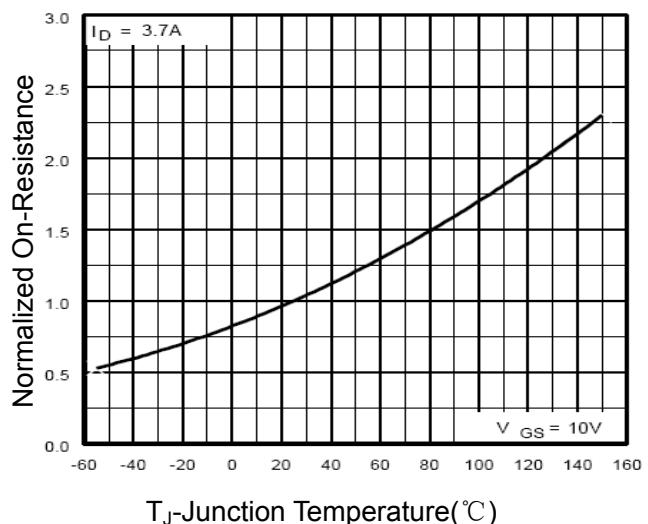


Figure 4 Rdson-JunctionTemperature

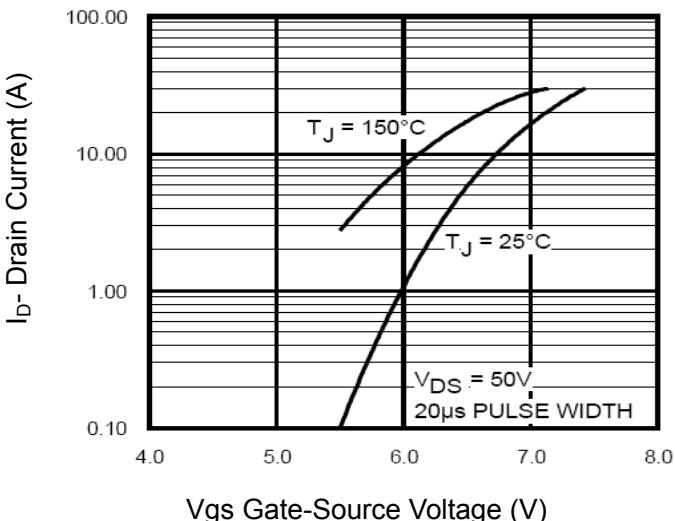


Figure 2 Transfer Characteristics

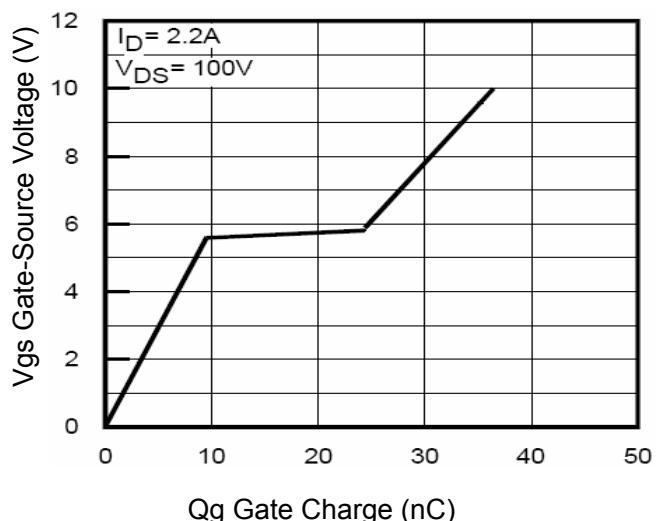


Figure 5 Gate Charge

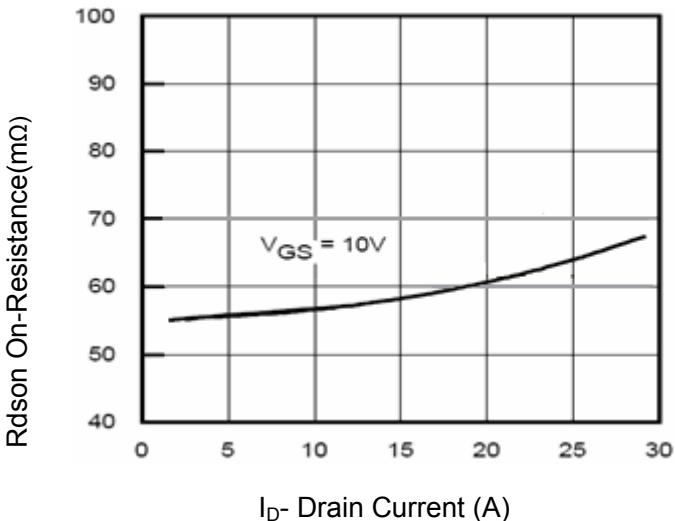


Figure 3 Rdson- Drain Current

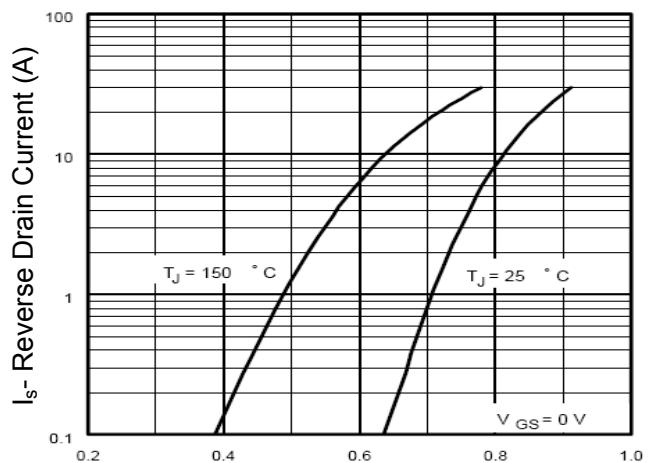


Figure 6 Source- Drain Diode Forward

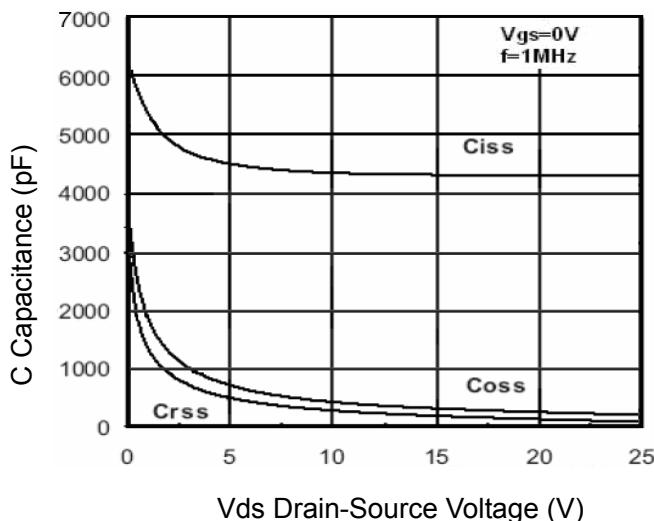


Figure 7 Capacitance vs Vds

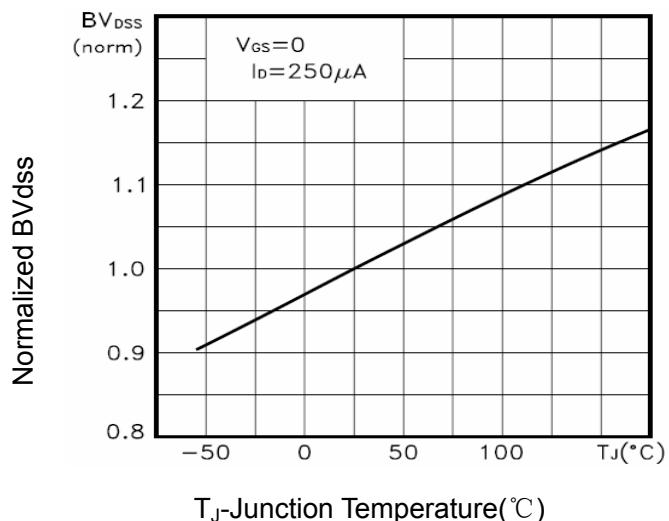


Figure 9 BV_{dss} vs Junction Temperature

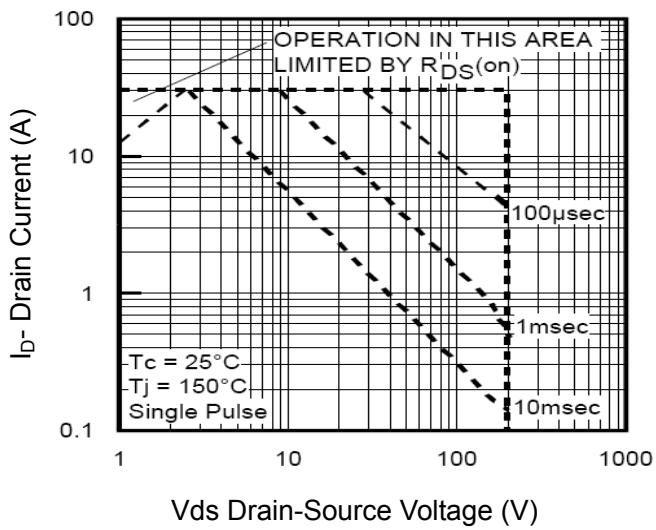


Figure 8 Safe Operation Area

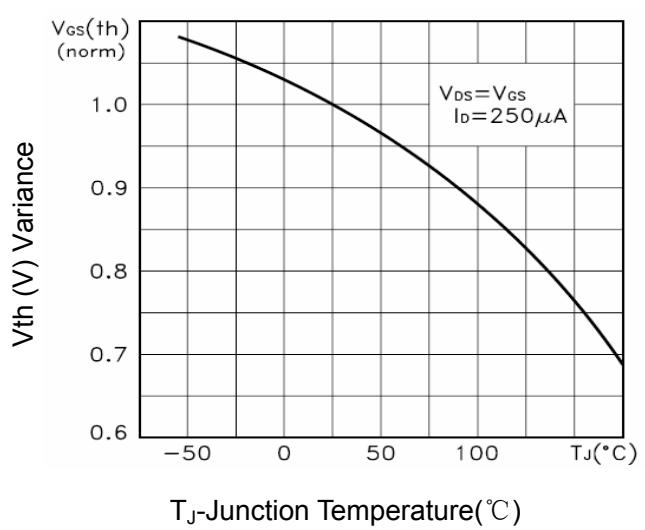


Figure 10 $V_{gs(th)}$ vs Junction Temperature

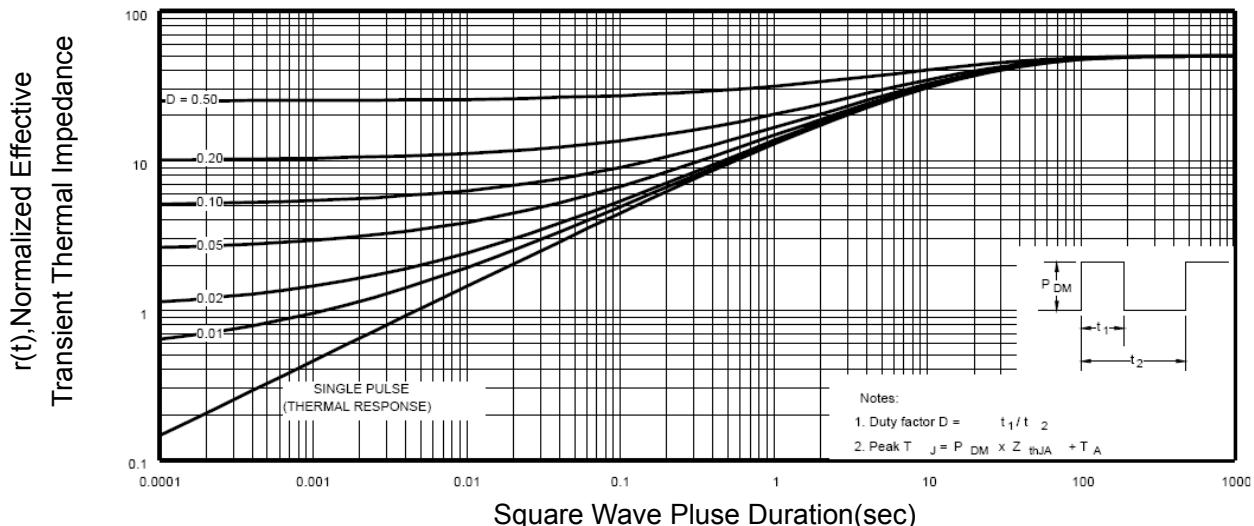
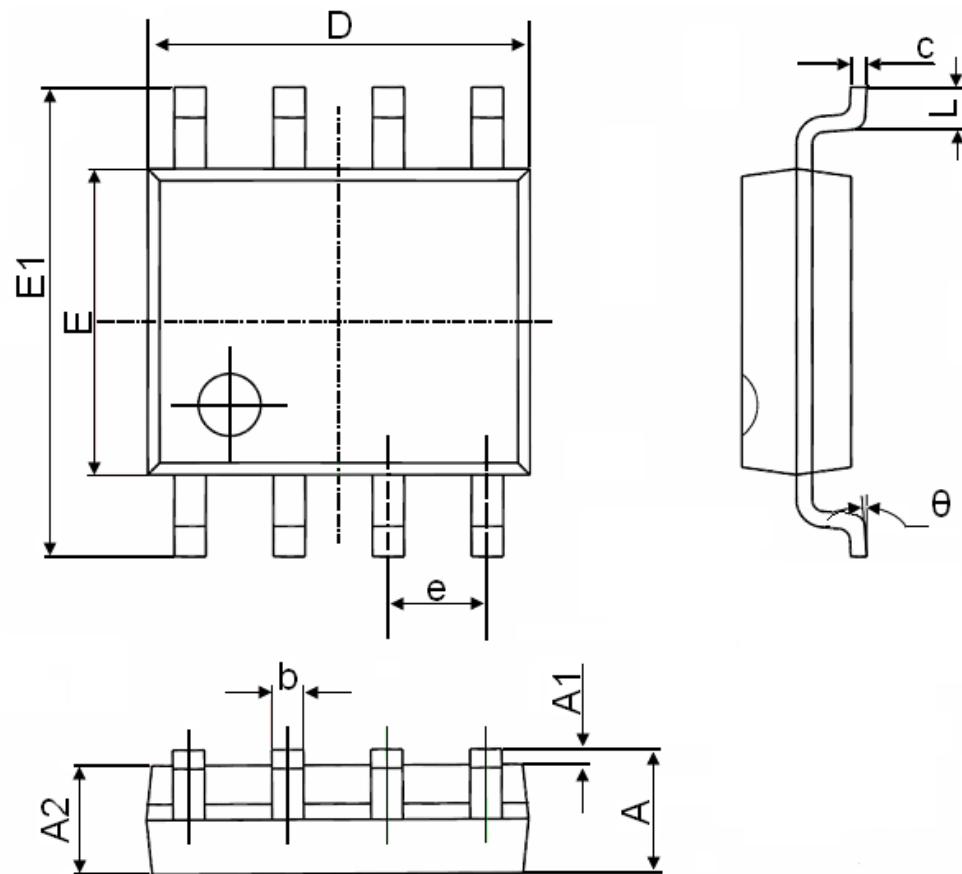


Figure 11 Normalized Maximum Transient Thermal Impedance

SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°