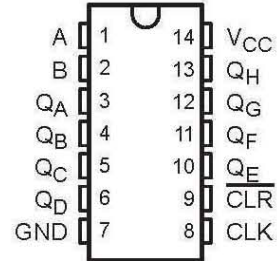


- Wide Operating Voltage Range of 2 V to 6V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical t_{pd} =20 ns
- ± 4 -mA Output Drive at 5V
- Low Input Current of 1 μ A Max
- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Direct Clear

PT Ĩ Ĩ PÔĤ Ĩ Ĩ ...AD,N,NS, OR PW PACKAGE
(TOP VIEW)



Description/ordering information

These 8-bit shift registers feature AND-gated serial inputs and an asynchronous clear (CLR) input. The gated serial (A and B) input permit complete control over incoming data; a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock (CLK) pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs can be changed while CLK is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of CLK.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PARTNUMBER	TOP-SIDE MARKING
-40 to 85	PDIP –AN	Tube of 25	HM74HC164AN	HM74HC164AN
	PDIP –N	Tube of 25	HM74HC164N	HM74HC164N
	SOIC - D	Tube of 50	HM74HC164AD	HC164
		Reel of 2500	HM74HC164AD	
		Reel of 250	HM74HC164DT	
	SOP –NS	Reel of 2000	HM74HC164NSR	HC164
	TSSOP – PW	Tube of 90	HM74HC164PW	HC164
		Reel of 2000	HM74HC164PWR	
		Reel of 250	HM74HC164PWT	

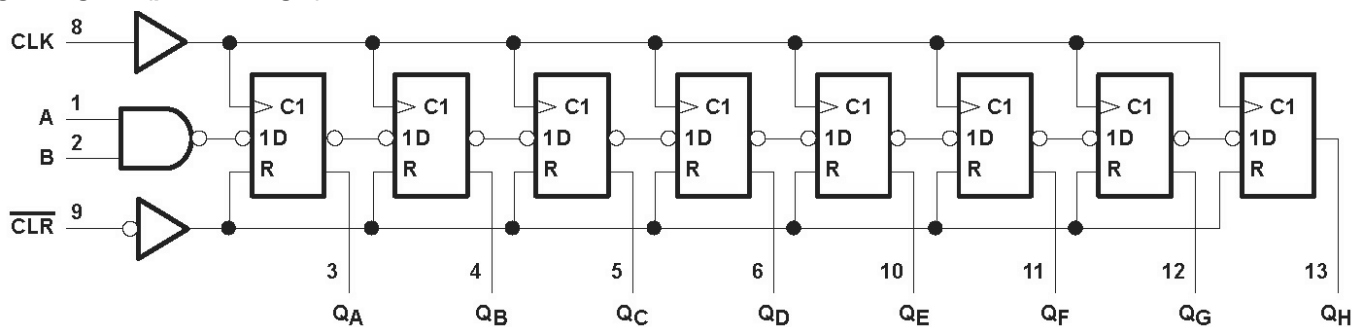
FUNCTION TABLE

INPUTS				OUTPUTS		
$\overline{\text{CLR}}$	CLK	A	B	Q_A	$Q_B \dots Q_H$	
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B , or Q_H , respectively,
before the indicated steady-state input conditions were
established

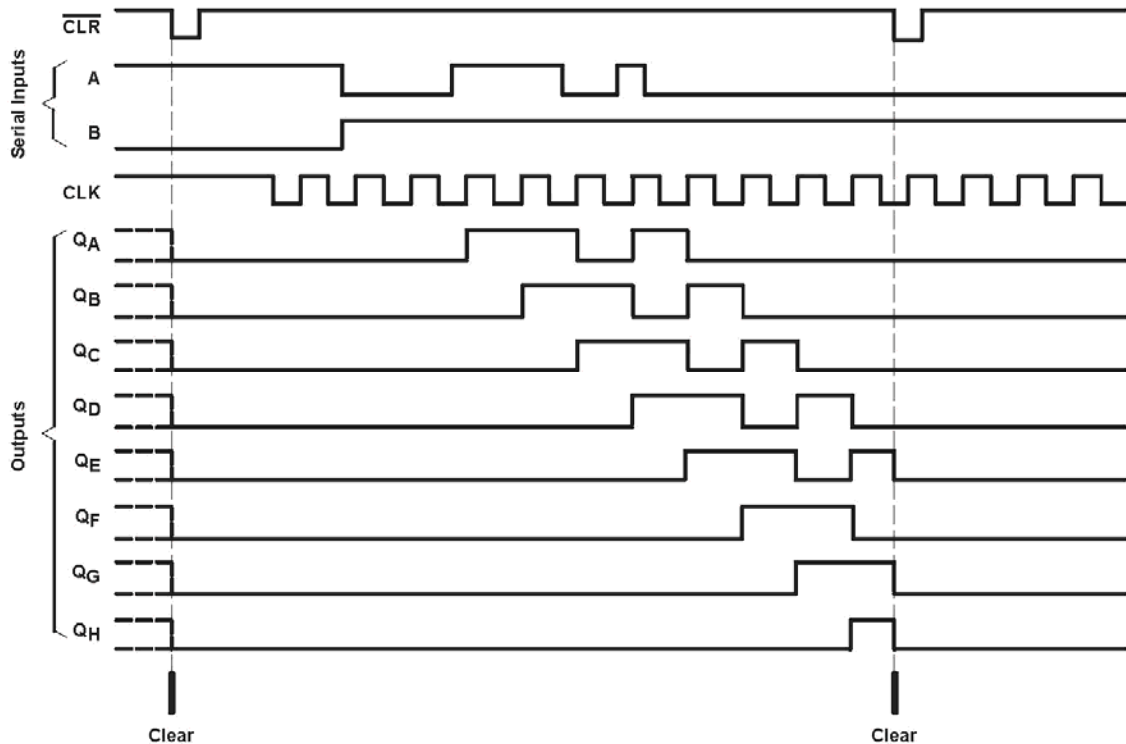
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent
↑ transition of CLK: indicates a 1-bit shift

logic diagram (positive logic)



Pin numbers shown are for the AD,J,N,NS, PW, and W packages.

Typical clear, shift, and clear sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted) †

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, $I_{IK}(V_I < 0 \text{ or } V_I > V_{CC})$ (see Note 1).....	$\pm 20\text{mA}$
Output clamp current, $I_{OK}(V_O < 0 \text{ or } V_O > V_{CC})$ (see Note 1).....	$\pm 20\text{mA}$
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	$\pm 25\text{mA}$
Continuous current through V_{CC} or GND.....	$\pm 50\text{mA}$
Package thermal impedance, θ_{JA} (see Note 2): AD package.....	86 /W
N package.....	80 /W
NS package.....	76 /W
PW package.....	113 /W
Storage temperature range, T_{stg}	-65 to 150

†Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7

Recommended operating conditions (see Note 3)

			PT Ĩ Ĩ PÔ Ĩ Ĩ			MIN PT Ĩ Ĩ PÔ Ĩ Ĩ			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		2	5	6	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} =2V	1.5			1.5			V
		V _{CC} =4.5V	3.15			3.15			
		V _{CC} =6V	4.2			4.2			
V _{IL}	Low-level input voltage	V _{CC} =2V			0.5			0.5	V
		V _{CC} =4.5V			1.35			1.35	
		V _{CC} =6V			1.8			1.8	
V _I	Input voltage		0		V _{CC}	0		V _{CC}	V
V _O	Output voltage		0		V _{CC}	0		V _{CC}	V
t / v†	Input transition rise/fall time	V _{CC} =2V			1000			1000	ns
		V _{CC} =4.5V			500			500	
		V _{CC} =6V			400			400	
T _A	Operating free-air temperature		-55		125	-40		85	

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report. Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

† If this device is used in the threshold region (from V_{IL} max = 0.5V to V_{IH} min = 1.5V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t₁ = 1000ns and V_{CC} = 2V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A =25			HM54HC164		HM74HC164		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2V	1.9	1.998		1.9		1.9		V
			4.5V	4.4	4.499		4.4		4.4		
			6V	5.9	5.999		5.9		5.9		
		I _{OH} = -4mA	4.5V	3.98	4.3		3.7		3.84		
		I _{OH} = -5.2mA	6V	5.48	5.8		5.2		5.34		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2V		0.002	0.1		0.1		0.1	V
			4.5V		0.001	0.1		0.1		0.1	
			6V		0.001	0.1		0.1		0.1	
		I _{OL} = 4mA	4.5V		0.17	0.26		0.4		0.33	
		I _{OL} = 5.2mA	6V		0.15	0.26		0.4		0.33	
I _I	V _I = V _{CC} or 0		6V		± 0.1	± 100		± 1000		± 1000	nA
I _{CC}	V _I = V _{CC} or 0, I _O = 0		6V			8		160		80	μA
C _i			2V to 6V		3	10		10		10	pF

Timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V _{CC}	T _A =25		HM54HC164AN		HM74HC164AN		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	2V		6		4.2		5	MHz
		4.5V		31		21		25	
		6V		36		25		28	
t _w	$\overline{\text{CLR}}$ low	2V	100		150		125		ns
		4.5V	20		30		25		
		6V	17		25		21		
	CLK high or low	2V	80		120		100		
		4.5V	16		24		20		
		6V	14		20		18		
t _{su}	Data	2V	100		150		125		ns
		4.5V	20		30		25		
		6V	17		25		21		
	$\overline{\text{CLR}}$ inactive	2V	100		150		125		
		4.5V	20		30		25		
		6V	17		25		21		
t _h	Hold time, data after CLK↑	2V	5		5		5		ns
		4.5V	5		5		5		
		6V	5		5		5		

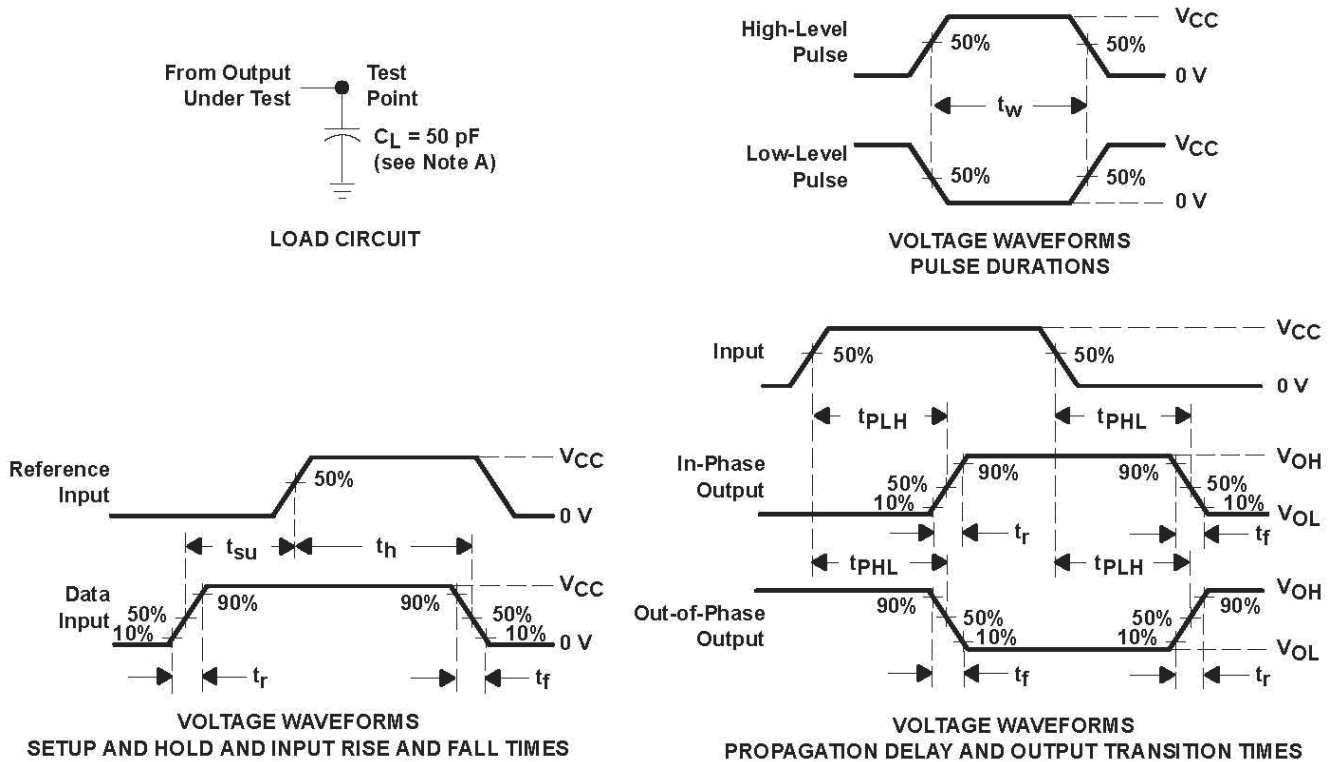
Switching characteristics over recommended operating free-air temperature range, CL = 50pF (unless otherwise noted)
(see Figure1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A =25			HM54HC164AN		HM74HC164AN		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			2V	6	10		4.2		5		MHz
			4.5V	31	54		21		25		
			6V	36	62		25		28		
t _{PHL}	$\overline{\text{CLR}}$	Any Q	2V		140	205		295		255	Ns
			4.5V		28	41		59		51	
			6V		24	35		51		46	
t _{pd}	CLK	Any Q	2V		115	175		265		220	
			4.5V		23	35		53		44	
			6V		20	30		45		38	
t _t			2V		38	75		110		95	ns
			4.5V		8	15		22		19	
			6V		6	13		19		16	

Operating characteristics, T_A = 25

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	No load	135	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.

B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR = 1MHz, $Z_O = 50 \Omega$, $t_r = 6\text{ns}$, $t_f = 6\text{ns}$.

C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.

D. The outputs are measured one at a time with one input transition per measurement.

E. t_{PLH} and t_{PHL} are the same as t_{pd} .

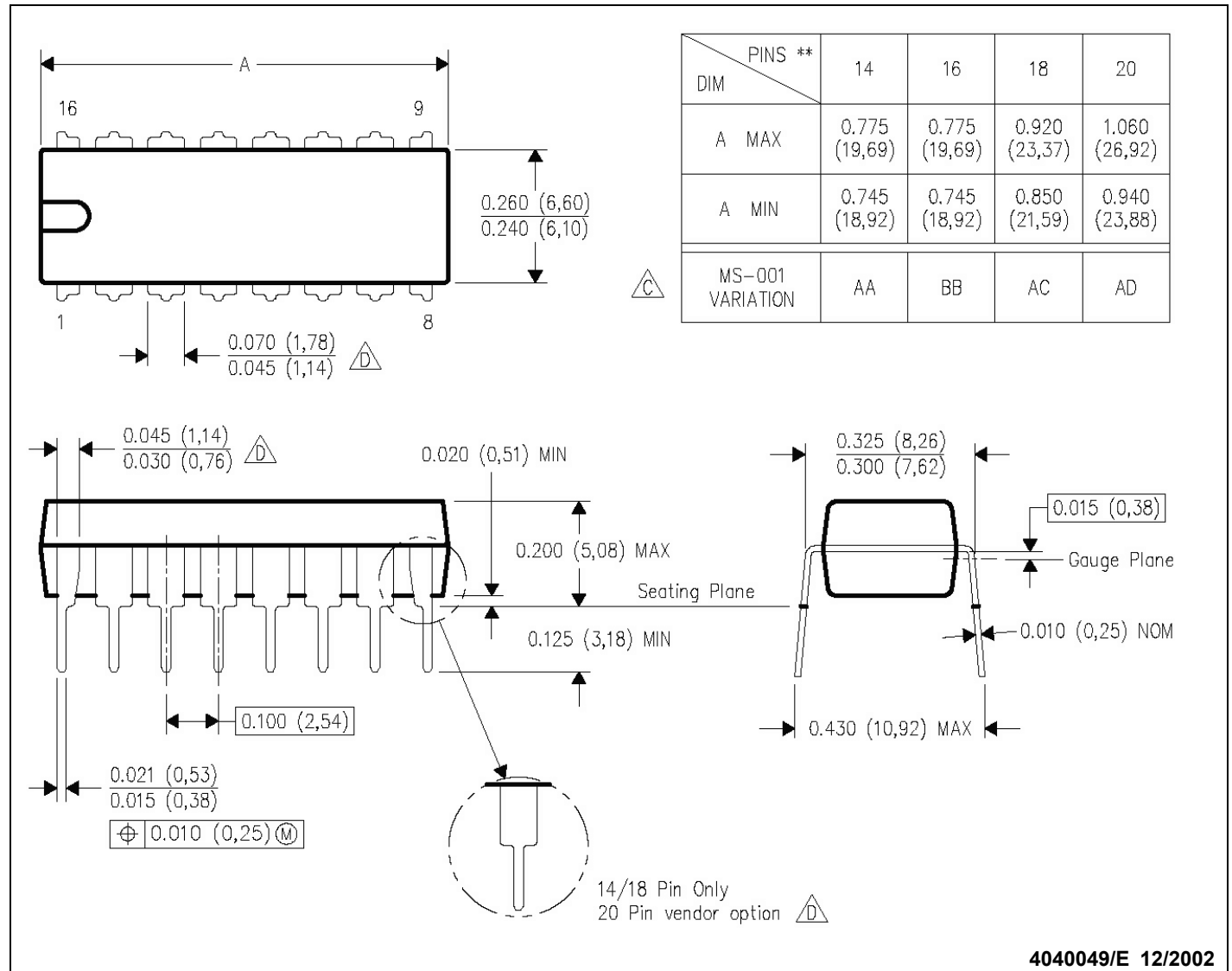
Figure 1. Load Circuit and Voltage Waveforms

MECHANICAL DATA

N (R-PDIP-T)**

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

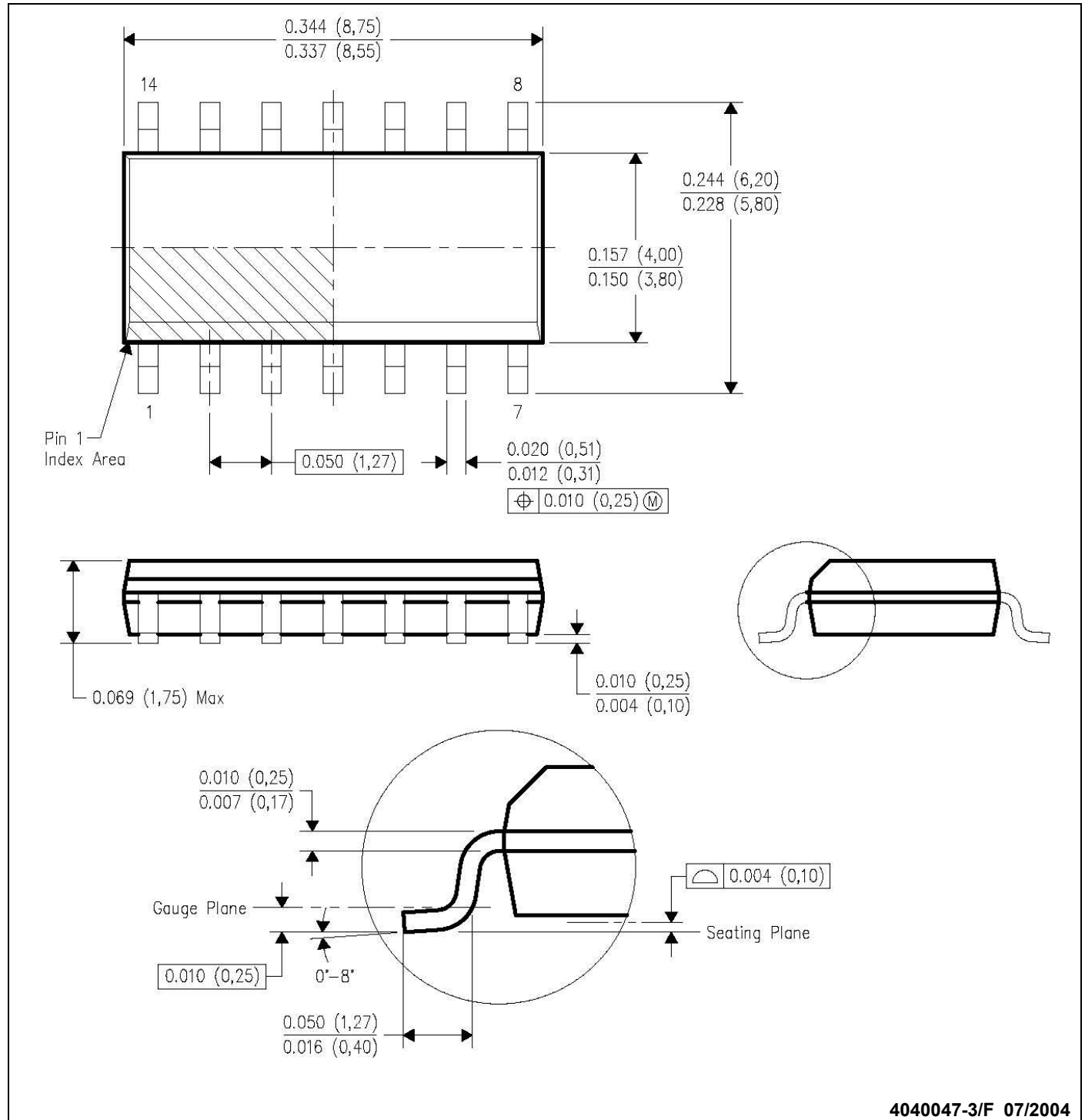
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

D (R-PDSO-G14)

PLASTIC

SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

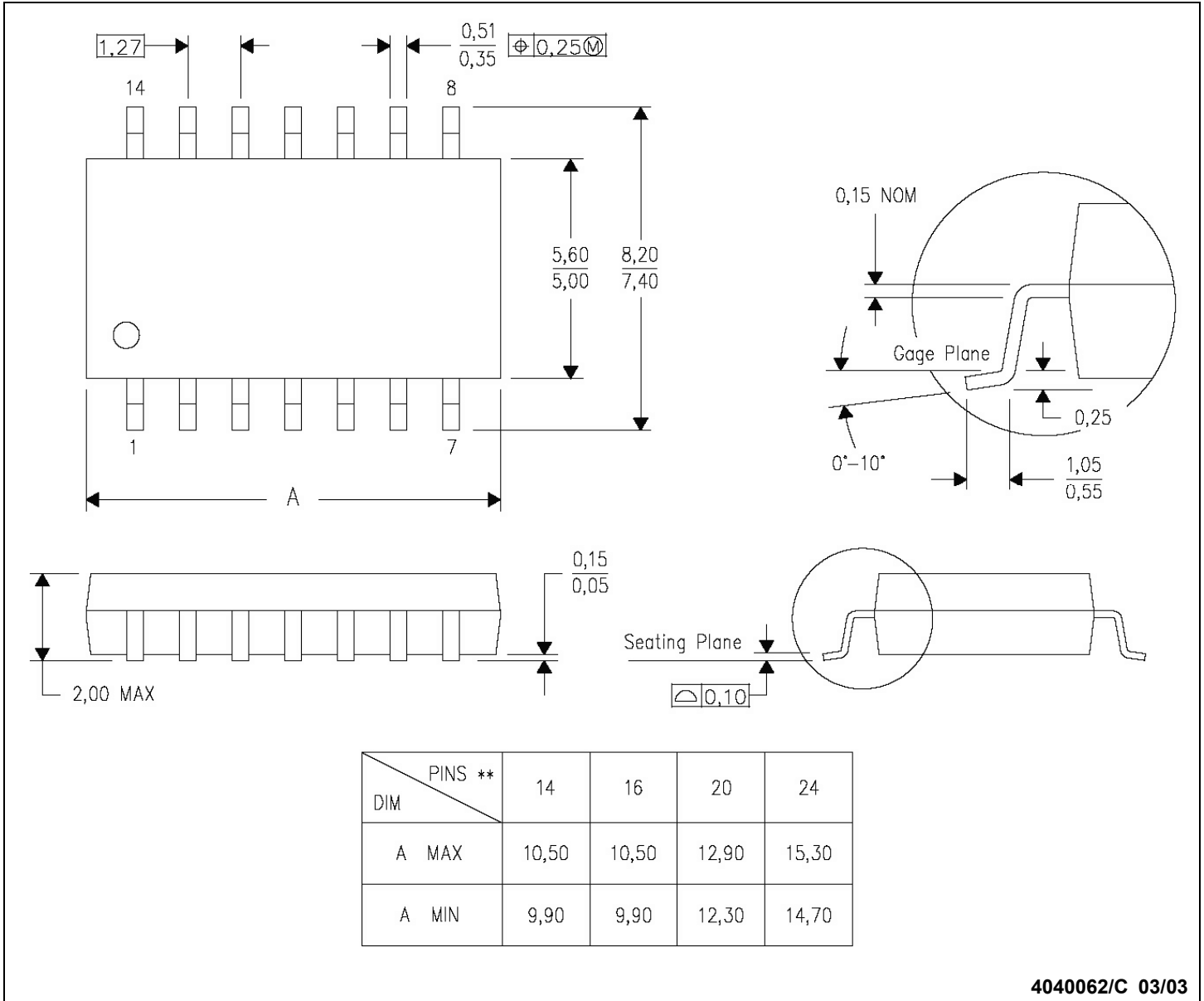
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).

D. Falls within JEDEC MS-012 variation AB.

MECHANICAL DATA

NS(R-PDSO-G)**
14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

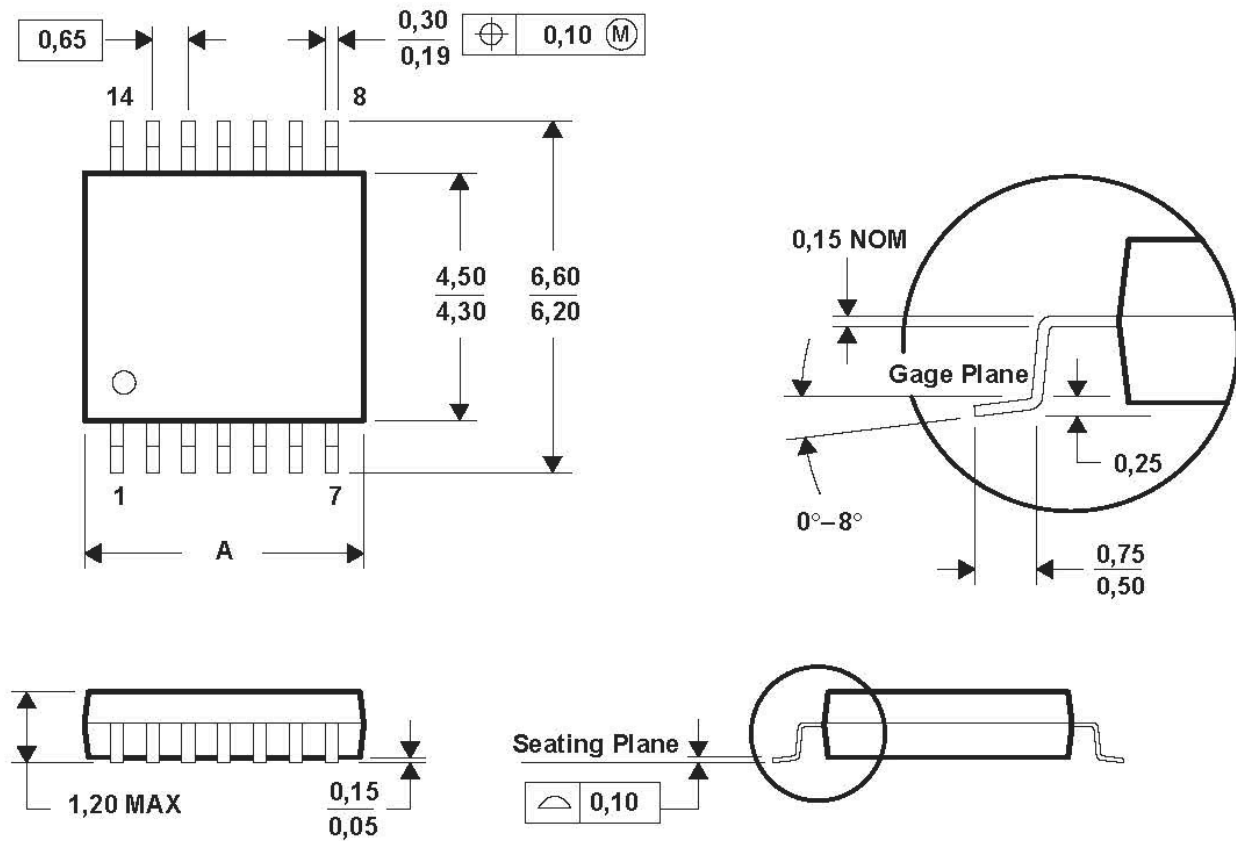
B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15.

PW (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

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- NOTES:** A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.15.
 D. Falls within JEDEC MO-153.