

## Description

The HM20N03Q uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

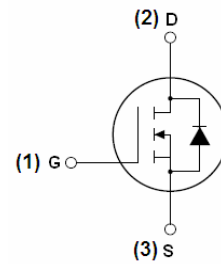
## General Features

- $V_{DS} = 30V, I_D = 20A$   
 $R_{DS(ON)} < 12.2m\Omega @ V_{GS} = 10V$   
 $R_{DS(ON)} < 20.5m\Omega @ V_{GS} = 5V$
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

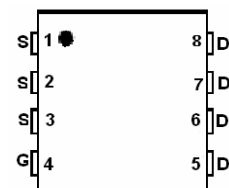
## Application

- Secondary side synchronous rectifier
- High side switch in POL DC/DC converter

**100% UIS TESTED!**



Schematic diagram



DFN 3x3 EP top view

## Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM20N03Q	HM20N03Q	DFN 3x3 EP	-	-	-

## Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	20	A
Pulsed Drain Current	$I_{DM}$	60	A
Maximum Power Dissipation	$P_D$	30	W
Derating factor		0.28	W/ $^\circ C$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	150	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ C$

## Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	3.6	°C/W
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## Electrical Characteristics (TC=25°C unless otherwise noted)

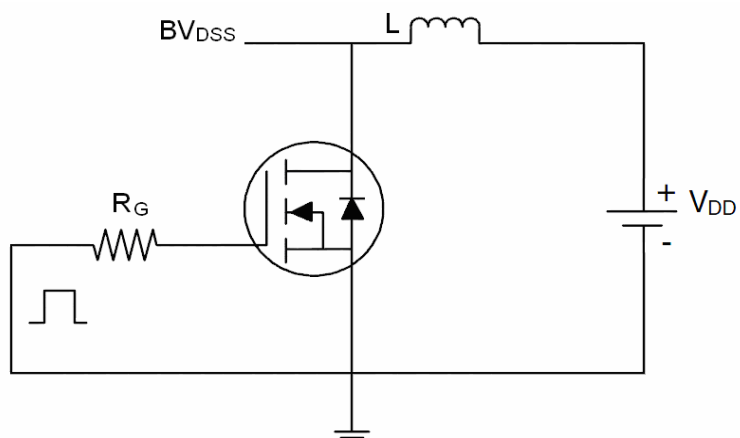
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	30	33	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics <sup>(Note 3)</sup>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1	1.7	2.2	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =12A	-	9.4	12.2	mΩ
		V <sub>GS</sub> =5V, I <sub>D</sub> =10A	-	15.8	20.5	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =12A	30	-	-	S
Dynamic Characteristics <sup>(Note4)</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, F=1.0MHz	-	1265	-	PF
Output Capacitance	C <sub>oss</sub>		-	600	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	130	-	PF
Switching Characteristics <sup>(Note 4)</sup>						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =15V, I <sub>D</sub> =12A V <sub>GS</sub> =10V, R <sub>GEN</sub> =6Ω	-	18	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	10	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	34	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	10	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =15V, I <sub>D</sub> =12A, V <sub>GS</sub> =10V	-	19	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	2.7	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	2.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <sup>(Note 3)</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =12A	-	0.85	1.2	V
Diode Forward Current <sup>(Note 2)</sup>	I <sub>S</sub>		-	-	20	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25°C, I <sub>F</sub> = 12A di/dt = 100A/μs(Note3)	-	-	47	nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	-	25	nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

## Notes:

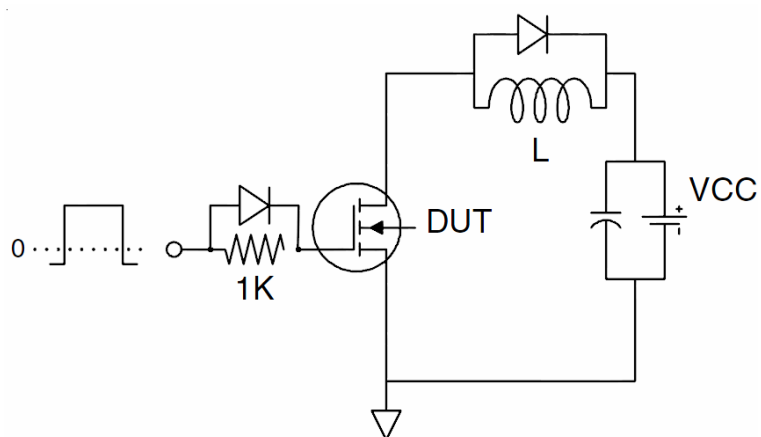
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition:  $T_J=25^\circ C, V_{DD}=15V, V_G=10V, L=0.1mH, R_g=25\Omega$

## Test Circuit

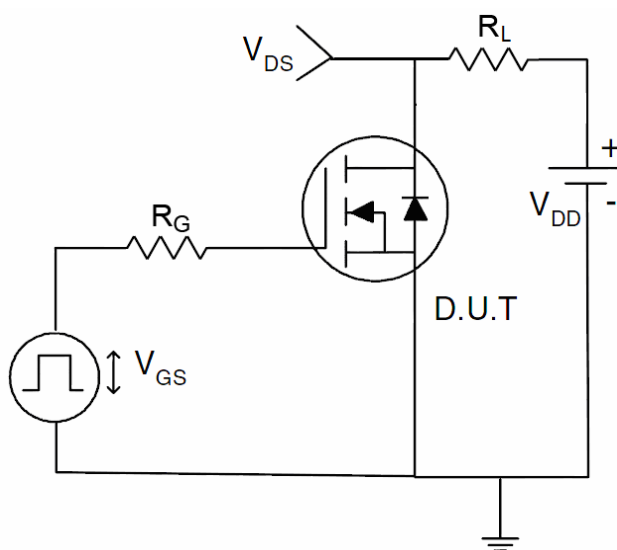
### 1) $E_{AS}$ Test Circuits



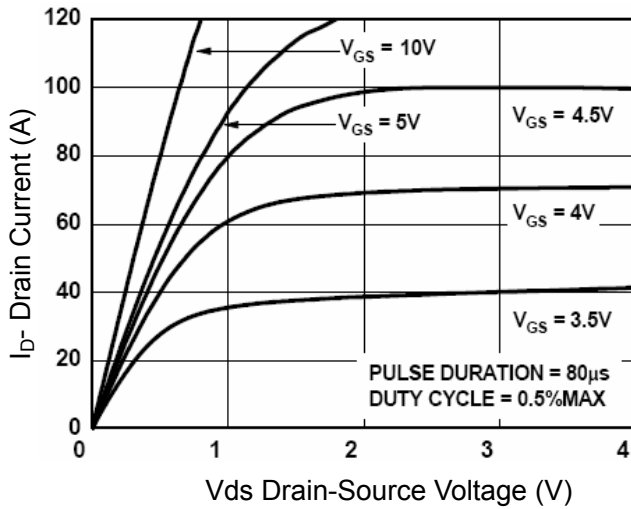
### 2) Gate Charge Test Circuit



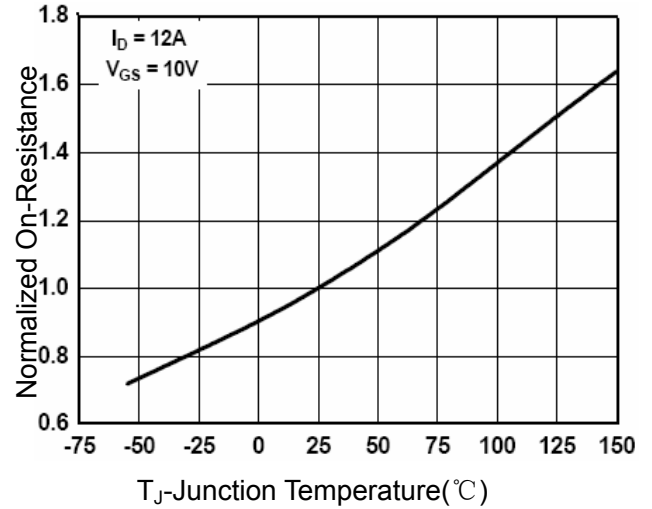
### 3) Switch Time Test Circuit



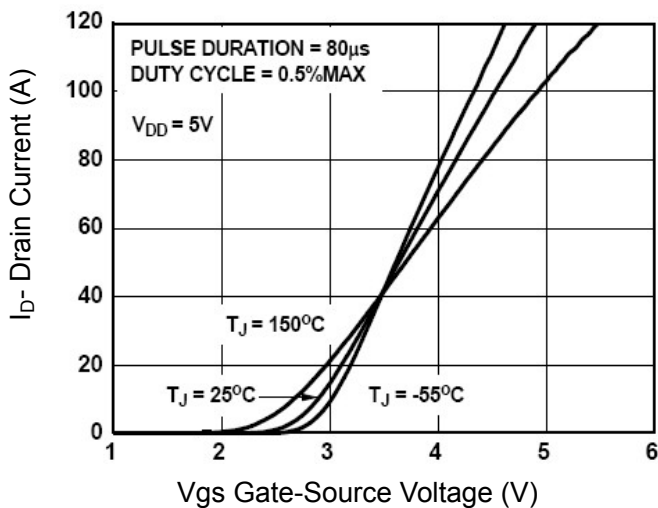
## Typical Electrical and Thermal Characteristics (Curves)



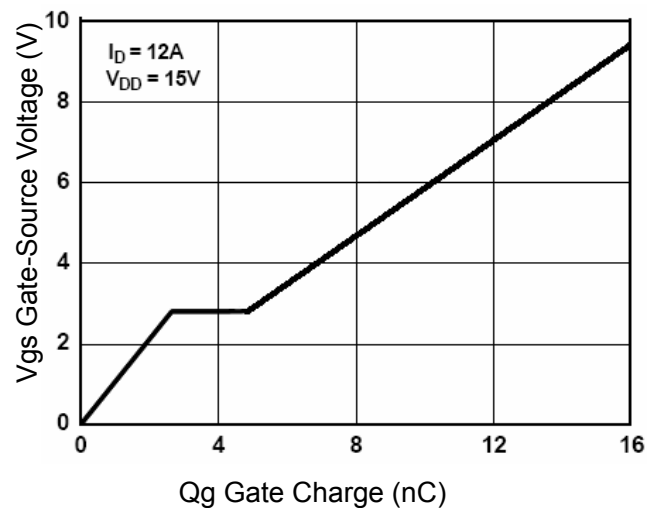
**Figure 1 Output Characteristics**



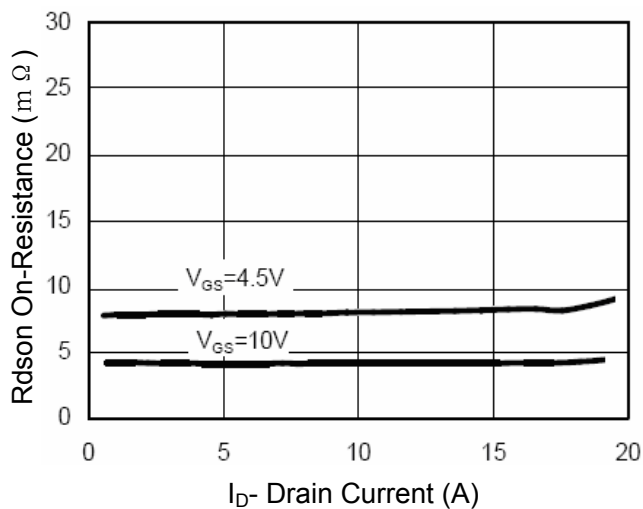
**Figure 4 Rdson-Junction Temperature**



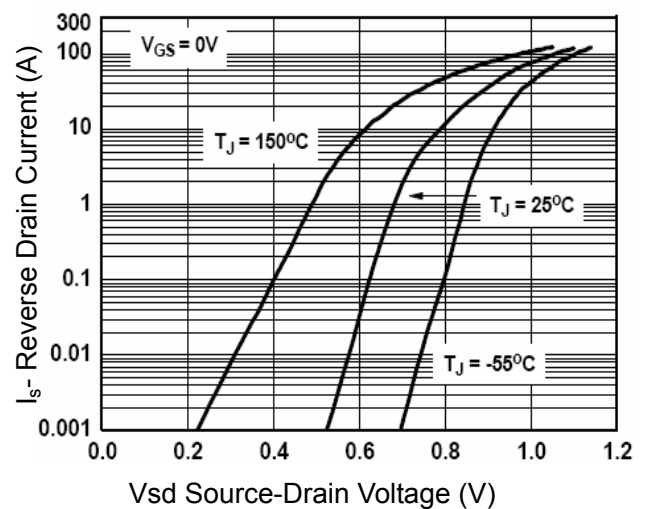
**Figure 2 Transfer Characteristics**



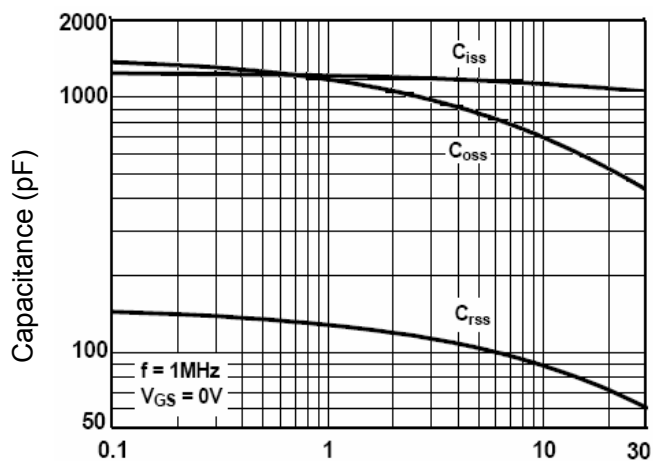
**Figure 5 Gate Charge**



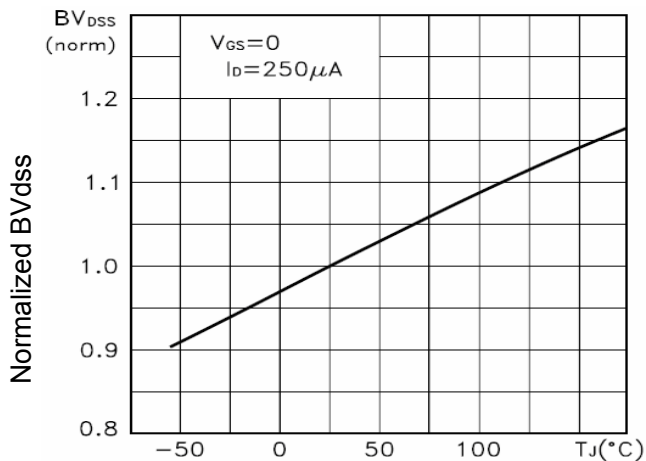
**Figure 3 Rdson- Drain Current**



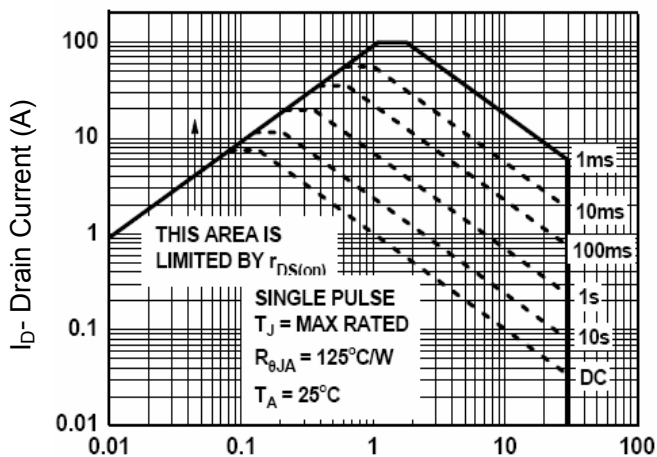
**Figure 6 Source- Drain Diode Forward**



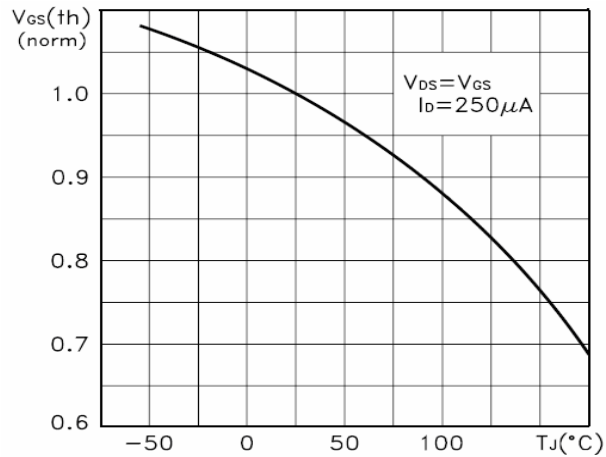
Vds Drain-Source Voltage (V)  
**Figure 7 Capacitance vs Vds**



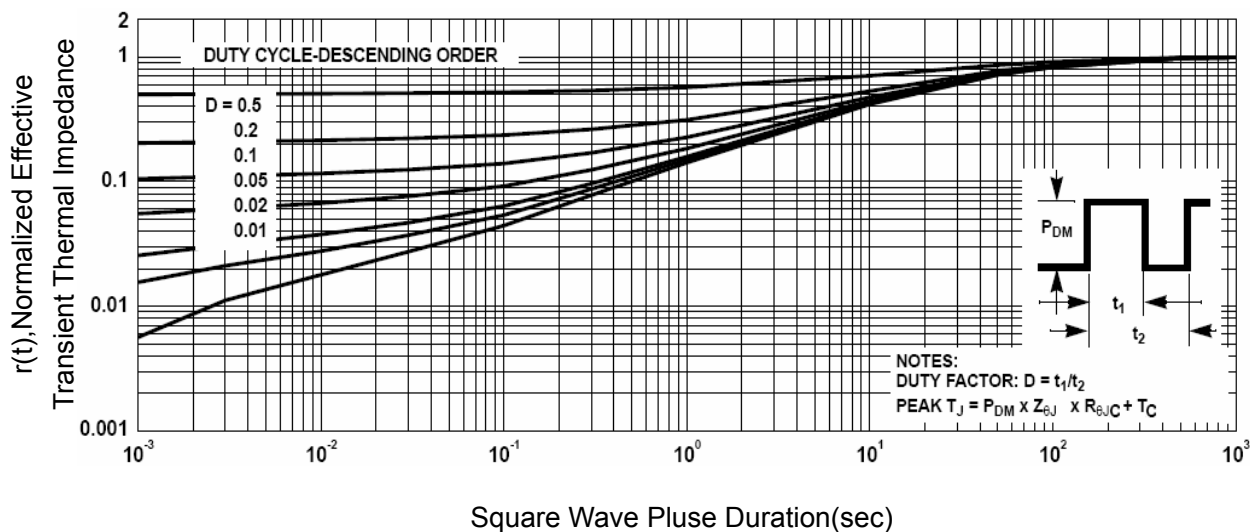
T<sub>J</sub>-Junction Temperature(°C)  
**Figure 9 BV<sub>DSS</sub> vs Junction Temperature**



Vds Drain-Source Voltage (V)  
**Figure 8 Safe Operation Area**

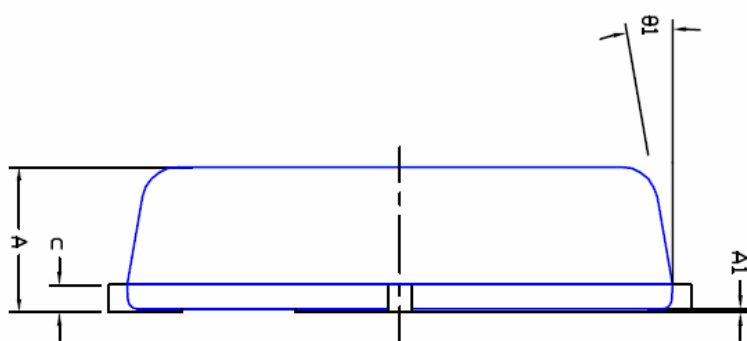
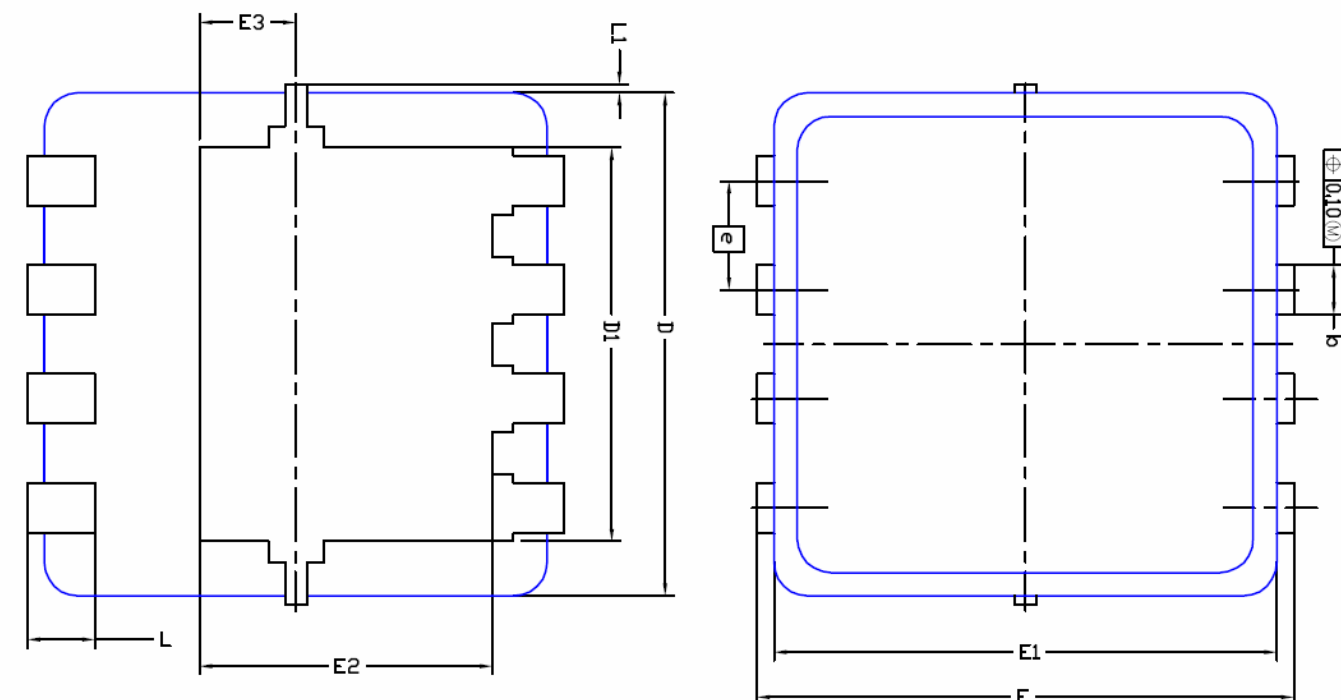


T<sub>J</sub>-Junction Temperature(°C)  
**Figure 10 V<sub>GS(th)</sub> vs Junction Temperature**



Square Wave Pluse Duration(sec)  
**Figure 11 Normalized Maximum Transient Thermal Impedance**

## DFN3X3 EP Package Information



DIM.	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.80	0.900	0.0276	0.0315	0.0354
A1	0.00	---	0.05	0.000	---	0.002
b	0.24	0.30	0.35	0.009	0.012	0.014
c	0.10	0.152	0.25	0.004	0.006	0.010
D	3.00 BSC			0.118 BSC		
D1	2.35 BSC			0.093 BSC		
E	3.20 BSC			0.126 BSC		
E1	3.00 BSC			0.118 BSC		
E2	1.75 BSC			0.069 BSC		
E3	0.575 BSC			0.023 BSC		
e	0.65 BSC			0.026 BSC		
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
L1	0	---	0.100	0	---	0.004
θ1	0°	10°	12°	0°	10°	12°