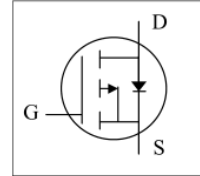


-300V P-Channel Enhancement Mode MOSFET

Description

The HM02P30PR uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



General Features

$V_{DS} = -300V$ $I_D = -0.2 A$

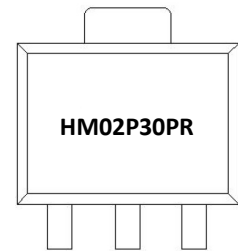
$R_{DS(ON)} < 17m\Omega$ @ $V_{GS}=10V$

Application

Battery protection

Load switch

Uninterruptible power supply



Marking and pin assignment

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
HM02P30PR	SOT-89	HM02P30PR	3000

Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-300	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_A = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ -10V^1$	-0.2	A
$I_D @ T_A = 70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ -10V^1$	-0.14	A
I_{DM}	Pulsed Drain Current ²	-0.6	A
$P_D @ T_A = 25^\circ\text{C}$	Total Power Dissipation ³	1	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹	125	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	80	$^\circ\text{C/W}$

-300V P-Channel Enhancement Mode MOSFET

Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=-250\mu A$	-300	---	---	V
$\Delta BVDSS/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=-1mA$	---	-0.0624	---	V/ $^{\circ}\text{C}$
RDS(ON) VGS(th)	Static Drain-Source On-Resistance ² Gate Threshold Voltage	$V_{GS}=-10V$, $I_D=-0.2A$	---	---	17	m Ω
		$V_{GS}=-4.5V$, $I_D=-0.2A$	---	---	---	
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient	$V_{GS}=V_{DS}$, $I_D=-250\mu A$	---	4.5	---	mV/ $^{\circ}\text{C}$
IDSS	Drain-Source Leakage Current	$V_{DS}=-80V$, $V_{GS}=0V$, $T_J=25^{\circ}\text{C}$	---	---	10	μA
		$V_{DS}=-80V$, $V_{GS}=0V$, $T_J=55^{\circ}\text{C}$	---	---	100	
IGSS	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=-5V$, $I_D=-0.8A$	---	3	---	S
R _g	Gate Resistance	$V_{DS}=0V$, $V_{GS}=0V$, $f=1MHz$	---	16	32	Ω
Q _g	Total Gate Charge (-4.5V)	$V_{DS}=-15V$, $V_{GS}=-4.5V$, $I_D=-0.5A$	---	4.5	---	nC
Q _{gs}	Gate-Source Charge		---	1.14	---	
Q _{gd}	Gate-Drain Charge		---	1.5	---	
T _{d(on)}	Turn-On Delay Time	$V_{DD}=-50V$, $V_{GS}=-10V$, $R_G=3.3\Omega$, $I_D=-0.5A$	---	13.6	---	ns
T _r	Rise Time		---	6.8	---	
T _{d(off)}	Turn-Off Delay Time		---	34	---	
T _f	Fall Time		---	3	---	
C _{iss}	Input Capacitance	$V_{DS}=-15V$, $V_{GS}=0V$, $f=1MHz$	---	553	---	pF
C _{oss}	Output Capacitance		---	29	---	
C _{rss}	Reverse Transfer Capacitance		---	20	---	
IS	Continuous Source Current ^{1,4}	$V_G=V_D=0V$, Force Current	---	---	-0.9	A
ISM	Pulsed Source Current ^{2,4}		---	---	-1.8	A
VSD	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=-1A$, $T_J=25^{\circ}\text{C}$	---	---	-1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch²FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The power dissipation is limited by 150°C junction temperature
- 4 .The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

-300V P-Channel Enhancement Mode MOSFET

Typical Characteristics

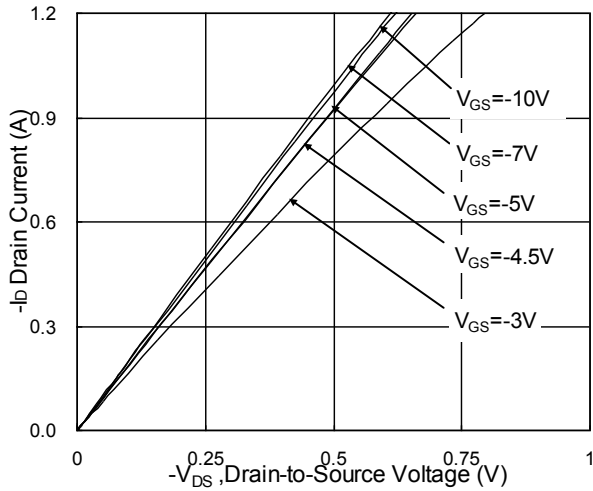


Fig.1 Typical Output Characteristics

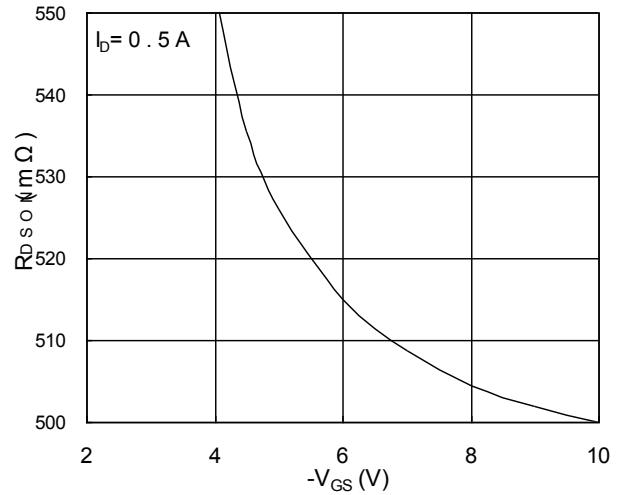


Fig.2 On-Resistance vs. Gate-Source

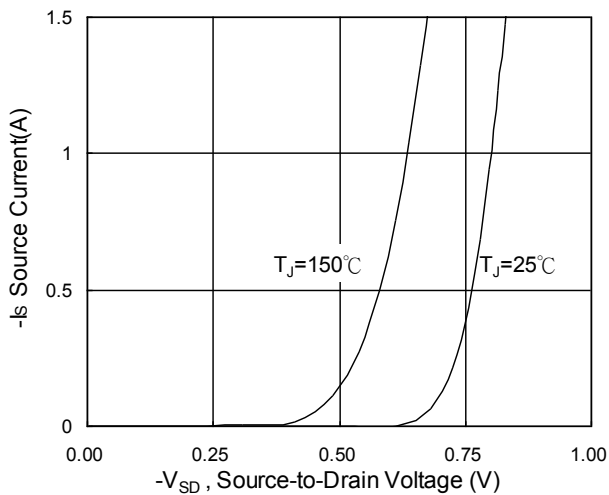


Fig.3 Forward Characteristics Of Reverse

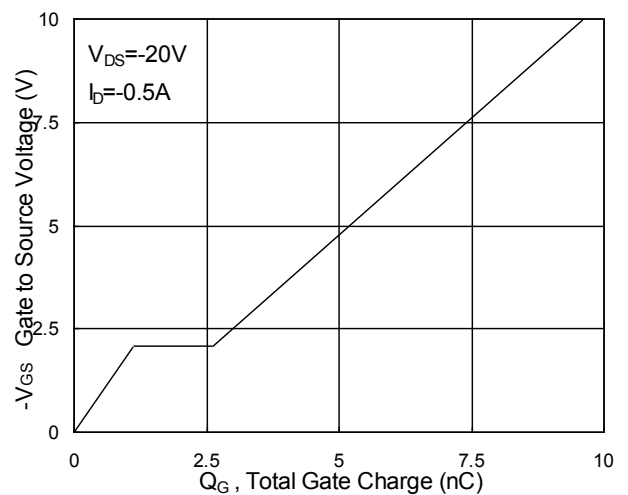


Fig.4 Gate-Charge Characteristics

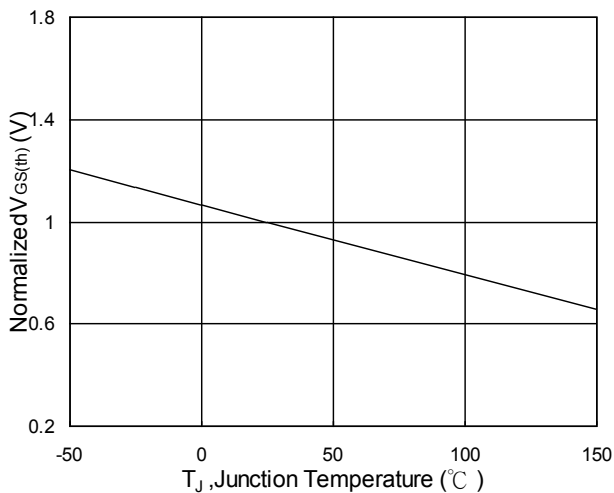


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

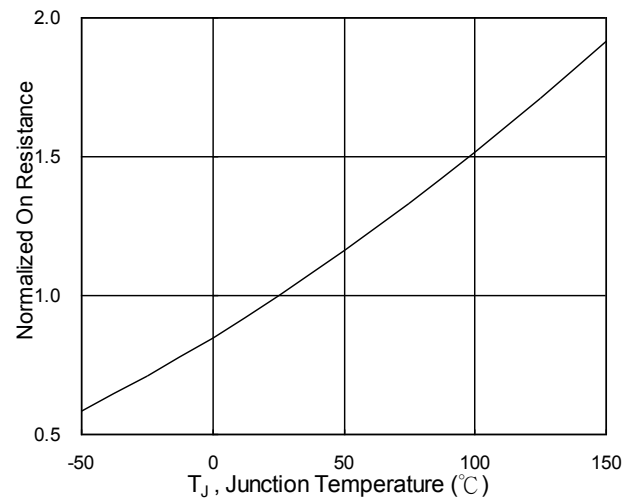


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

-300V P-Channel Enhancement Mode MOSFET

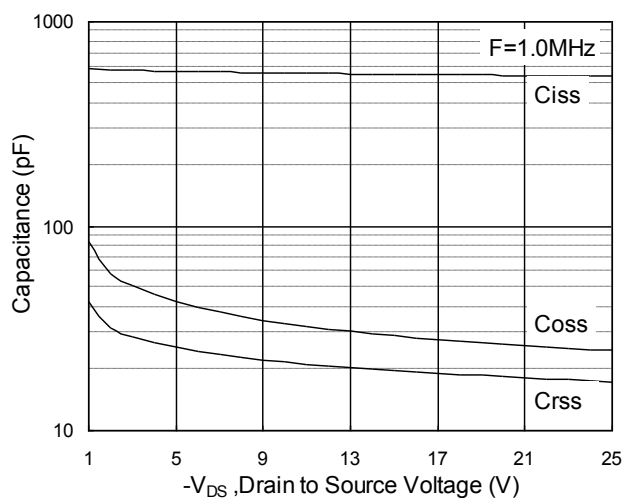


Fig.7 Capacitance

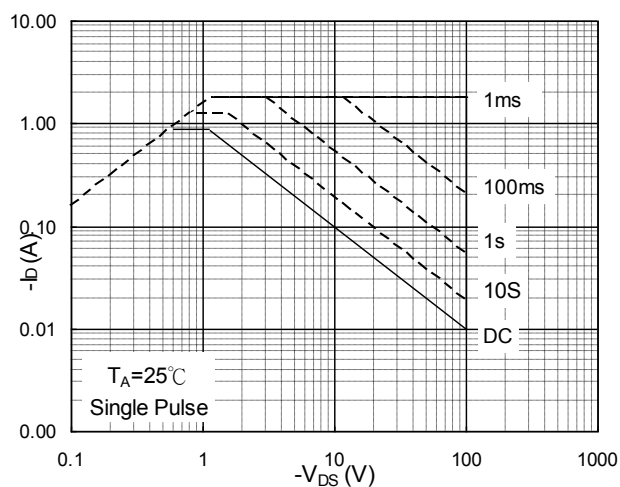


Fig.8 Safe Operating Area

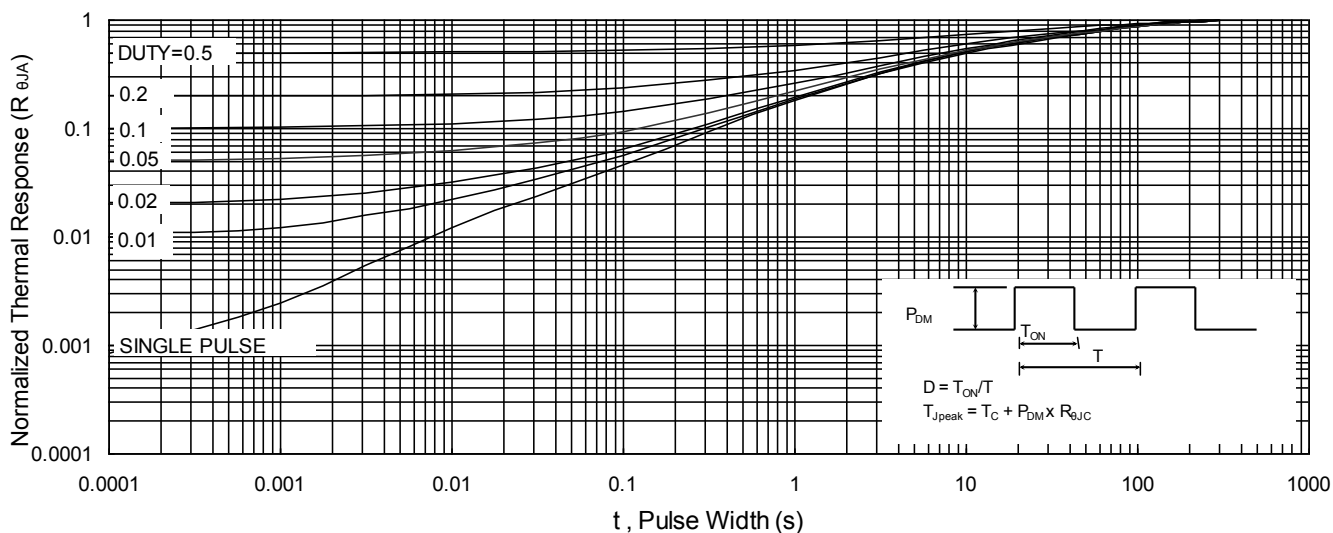


Fig.9 Normalized Maximum Transient Thermal Impedance

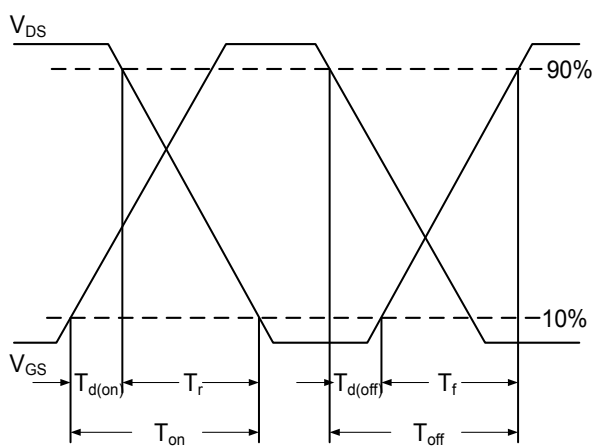


Fig.10 Switching Time Waveform

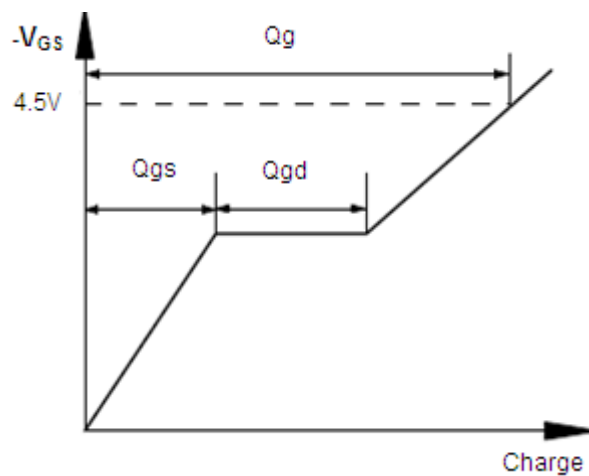
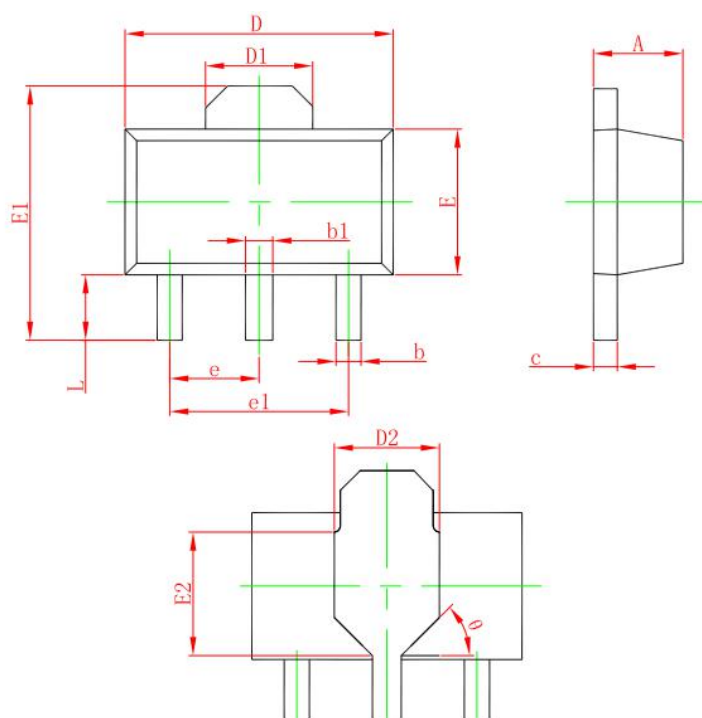


Fig.11 Gate Charge Waveform

Package Information:



Symbol	Dimensions in millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.020
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550REF		0.061REF	
D2	1.750 REF		0.069REF	
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
E2	1.900REF		0.075REF	
e	1.500TYP		0.060TYP	
e1	3.000TYP		0.118TYP	
L	0.900	1.200	0.035	0.047
θ	45°		45°	

SOT-89 Package