

P-Channel Enhancement Mode Power MOSFET

Description

The HM30P06D uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is well suited for high current load applications.

General Features

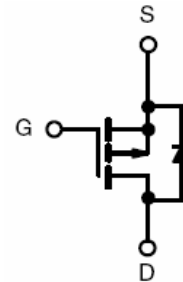
- $V_{DS} = -60V, I_D = -30A$
 $R_{DS(ON)} < 19.5m\Omega @ V_{GS} = -10V$
 $R_{DS(ON)} < 21.5m\Omega @ V_{GS} = -4.5V$
- High density cell design for ultra low $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

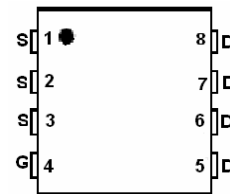
- Load switch

100% UIS TESTED!

100% ΔV_{ds} TESTED!



Schematic diagram



Marking and pin assignment

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM30P06D	HM30P06D	DFN5X6-8L	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-30	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	-21	A
Pulsed Drain Current	I_{DM}	-90	A
Maximum Power Dissipation	P_D	95	W
Derating factor		0.76	W/ $^\circ C$
Single pulse avalanche energy (Note 5)	E_{AS}	722	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	1.31	$^\circ C/W$
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Electrical Characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

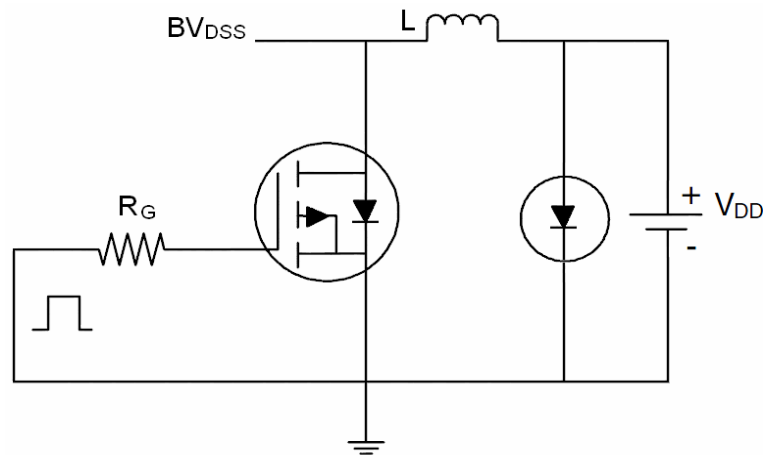
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V$ $I_D=-250\mu A$	-60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-60V, V_{GS}=0V$	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.1	-1.6	-2.1	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-20A$	-	17.0	19.5	m Ω
		$V_{GS}=-4.5V, I_D=-20A$	-	18.5	21.5	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=-10V, I_D=-10A$	-	25	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C_{iss}	$V_{DS}=-25V, V_{GS}=0V,$ $F=1.0MHz$	-	6460	-	PF
Output Capacitance	C_{oss}		-	719	-	PF
Reverse Transfer Capacitance	C_{rss}		-	535	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-30V, R_L=1.5\Omega,$ $V_{GS}=-10V, R_G=3\Omega$	-	15	-	nS
Turn-on Rise Time	t_r		-	17	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	40	-	nS
Turn-Off Fall Time	t_f		-	45	-	nS
Total Gate Charge	Q_g	$V_{DS}=-30, I_D=-10A,$ $V_{GS}=-10V$	-	75		nC
Gate-Source Charge	Q_{gs}		-	16		nC
Gate-Drain Charge	Q_{gd}		-	19		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_S=-10A$	-		-1.2	V
Diode Forward Current ^(Note 2)	I_S		-	-	-20	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}C, IF = -10A$ $di/dt = -100A/\mu s$ (Note3)	-	50		nS
Reverse Recovery Charge	Q_{rr}		-	59		nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

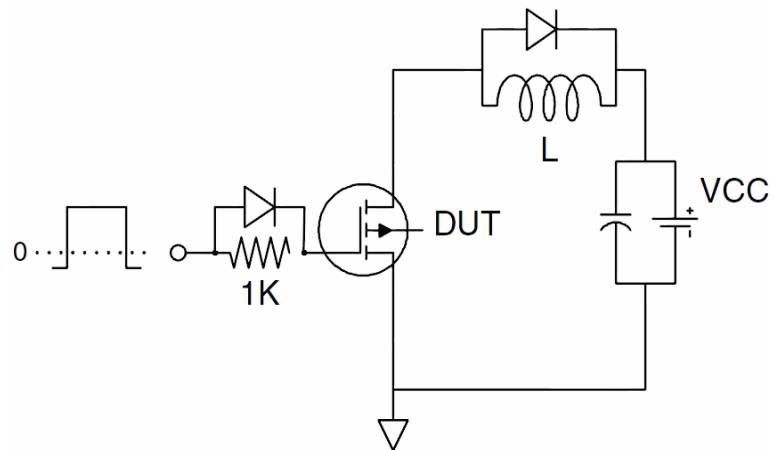
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. E_{AS} condition: $T_J=25^{\circ}\text{C}, V_{DD}=-20V, V_G=-10V, L=1mH, R_g=25\Omega, I_{AS}=38A$

Test Circuit

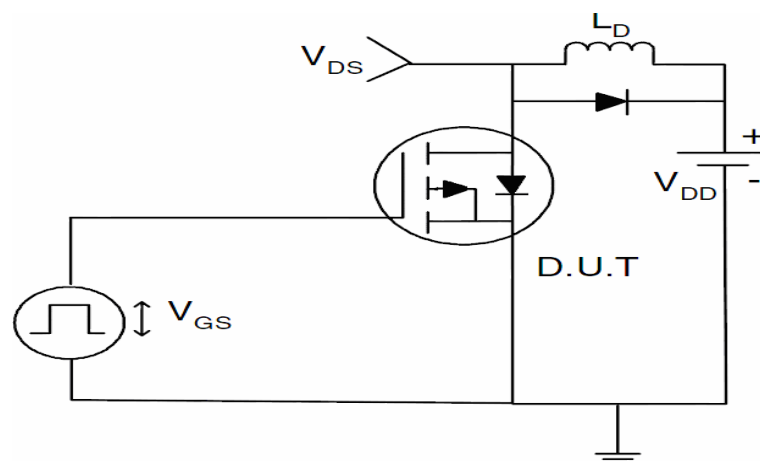
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

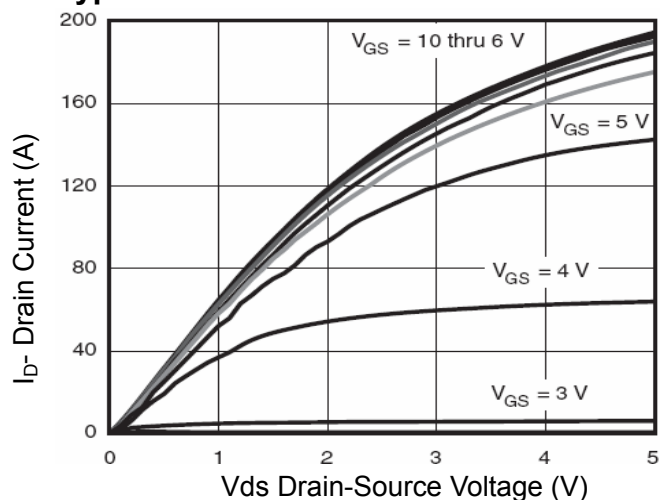


Figure 1 Output Characteristics

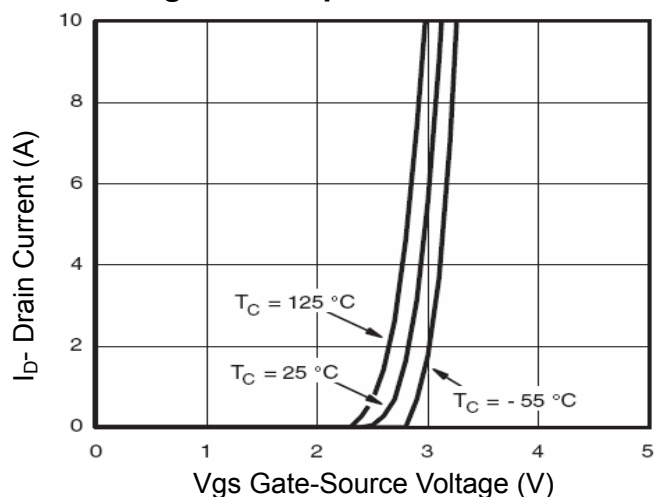


Figure 2 Transfer Characteristics

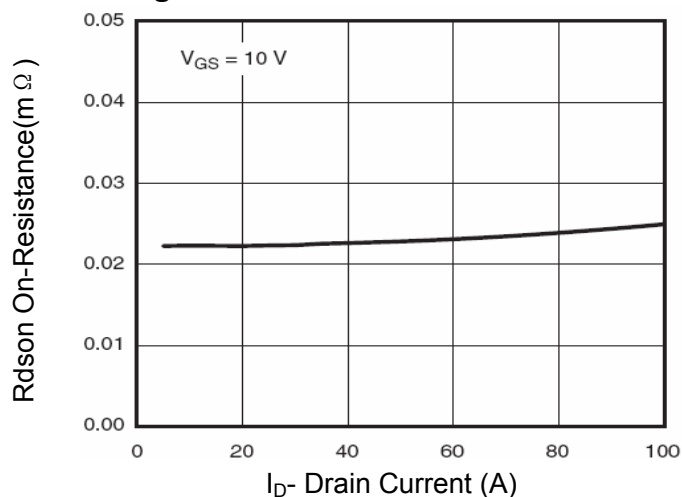


Figure 3 Rdson- Drain Current

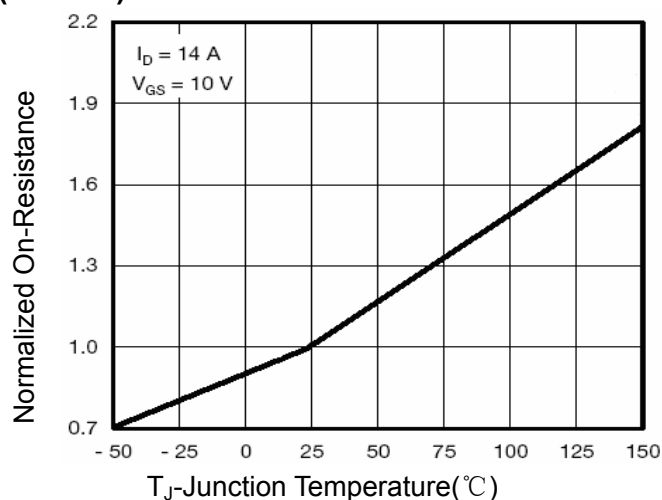


Figure 4 Rdson-Junction Temperature

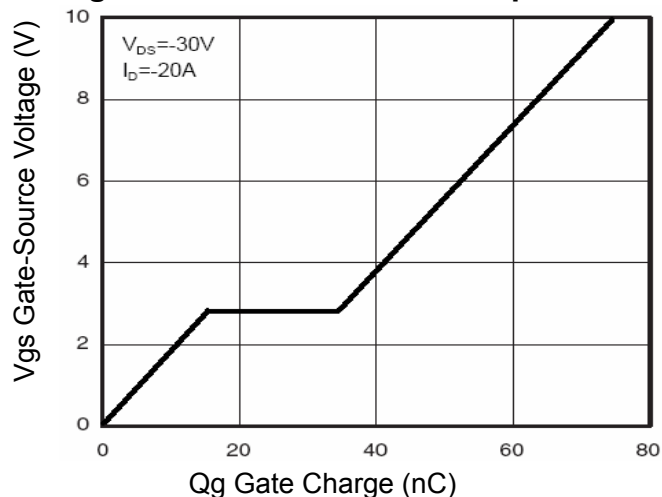


Figure 5 Gate Charge

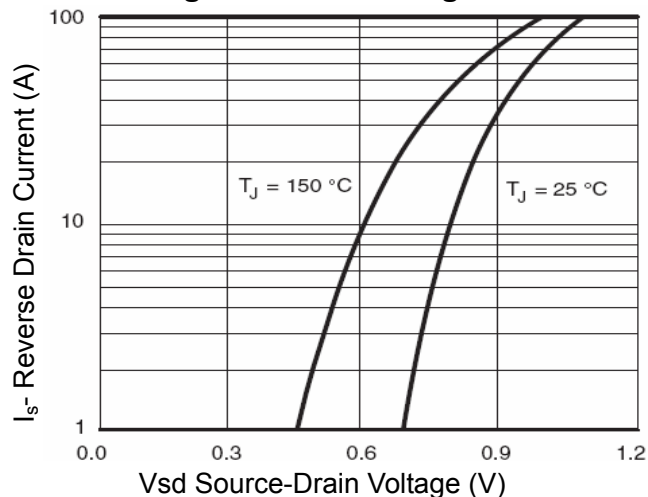


Figure 6 Source- Drain Diode Forward

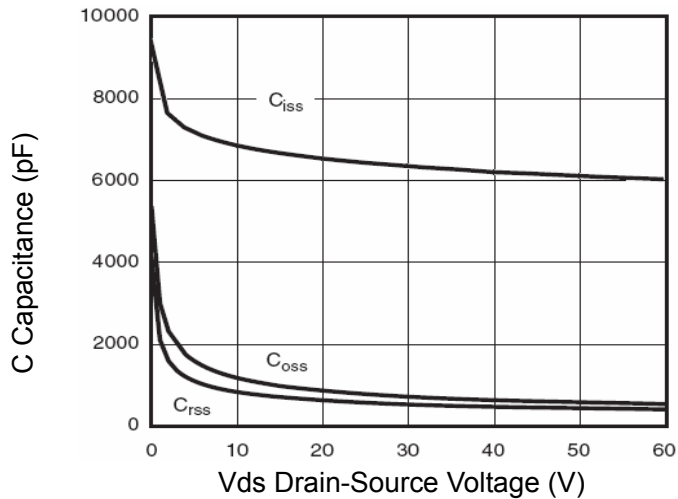


Figure 7 Capacitance vs Vds

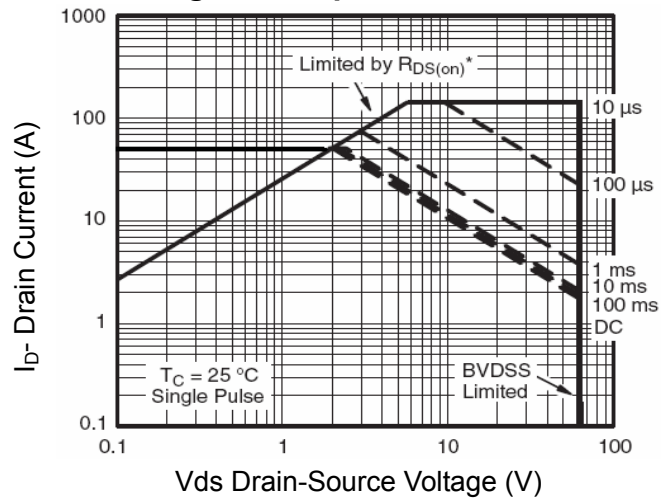


Figure 8 Safe Operation Area

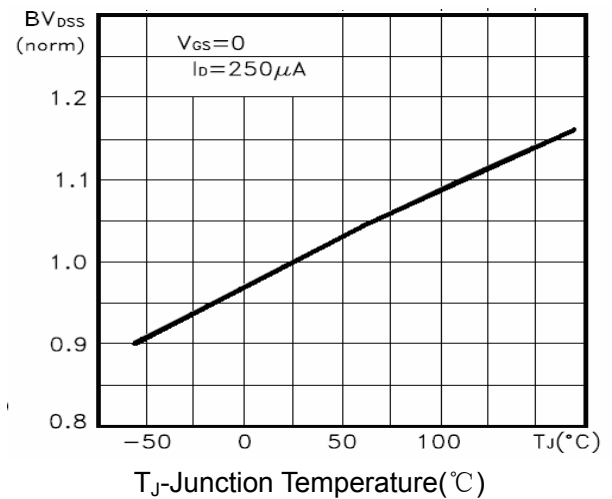


Figure 9 BV_{DSS} vs Junction Temperature

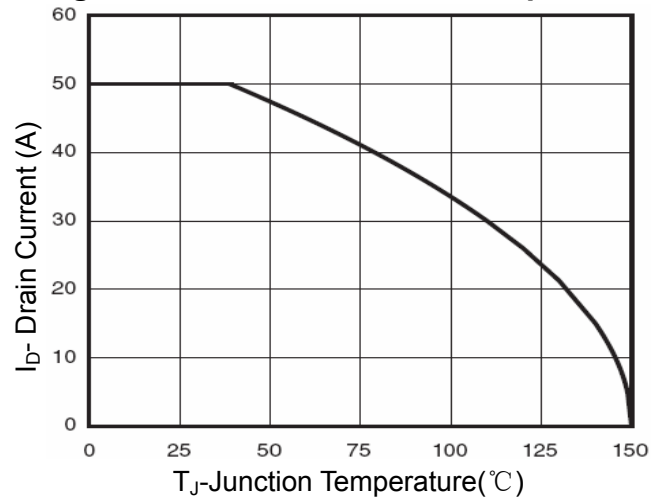


Figure 10 ID Current Derating vs Junction Temperature

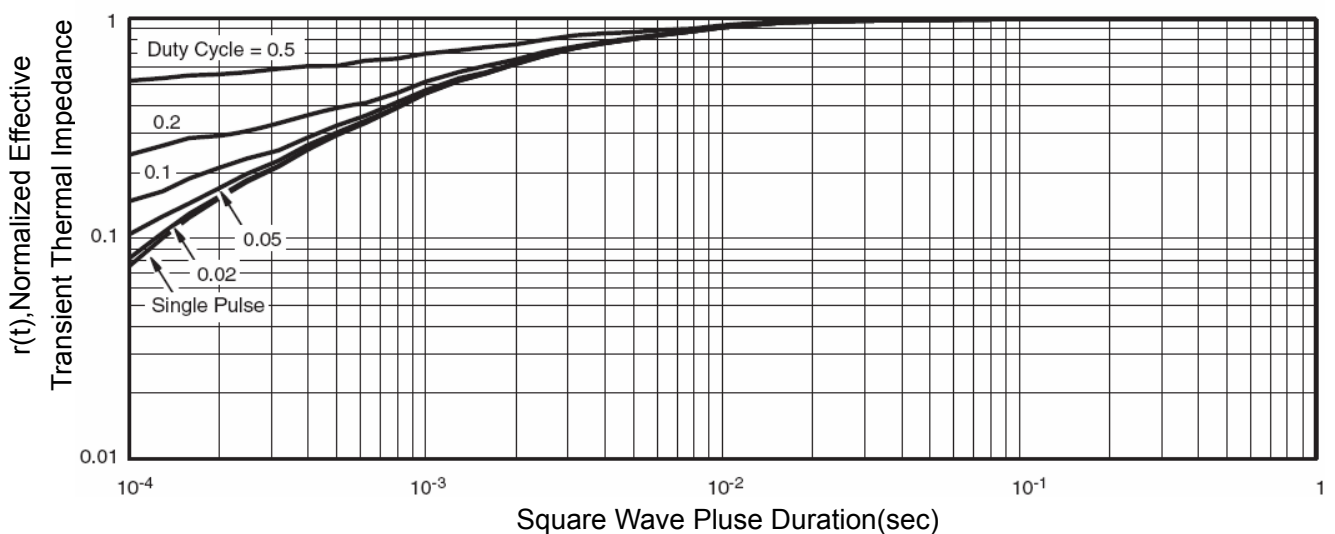
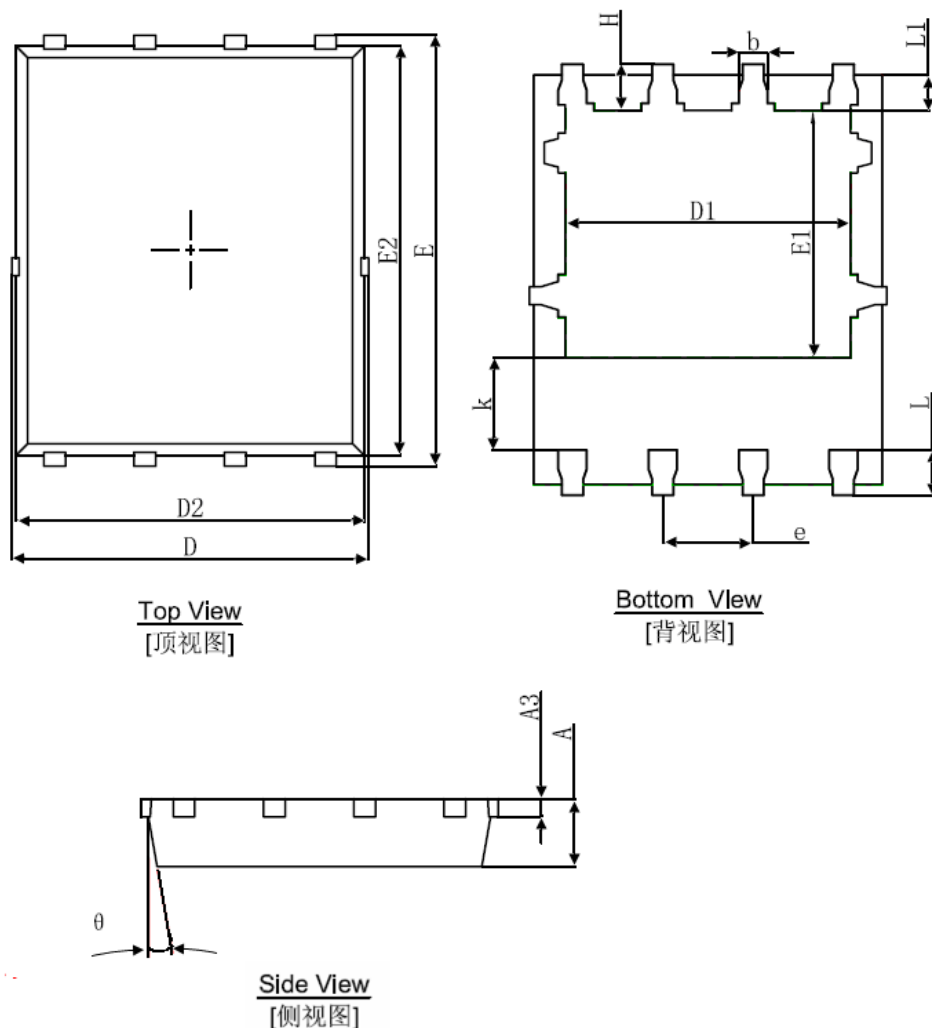


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	8°	12°	8°	12°

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