

N-Channel Enhancement Mode Power MOSFET

Description

The HM40N04Q uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

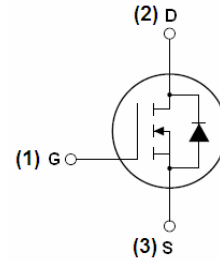
- $V_{DS} = 40V, I_D = 40A$
 $R_{DS(ON)} = 5.5m\Omega @ (Typ) V_{GS} = 10V$
- High density cell design for ultra low $R_{DS(ON)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

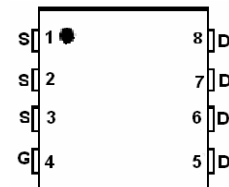
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

100% UIS TESTED!

100% ΔV_{ds} TESTED!



Schematic diagram



DFN3X3-8L top view

Package Marking and Ordering Information

| Device Marking | Device | Device Package | Reel Size | Tape width | Quantity |
|----------------|----------|----------------|-----------|------------|----------|
| HM40N04Q | HM40N04Q | DFN3X3-8L | - | - | - |

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

| Parameter | Symbol | Limit | Unit |
|---|---------------------|------------|---------------|
| Drain-Source Voltage | V_{DS} | 40 | V |
| Gate-Source Voltage | V_{GS} | ± 20 | V |
| Drain Current-Continuous | I_D | 40 | A |
| Drain Current-Continuous($T_C = 100^\circ C$) | $I_D (100^\circ C)$ | 28 | A |
| Pulsed Drain Current | I_{DM} | 120 | A |
| Maximum Power Dissipation | P_D | 65 | W |
| Derating factor | | 0.43 | W/ $^\circ C$ |
| Single pulse avalanche energy ^(Note 5) | E_{AS} | 400 | mJ |
| Operating Junction and Storage Temperature Range | T_J, T_{STG} | -55 To 175 | $^\circ C$ |

Thermal Characteristic

| | | | |
|--|-----------------|-----|----------------------|
| Thermal Resistance, Junction-to-Case ^(Note 2) | $R_{\theta JC}$ | 2.3 | $^{\circ}\text{C/W}$ |
|--|-----------------|-----|----------------------|

Electrical Characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

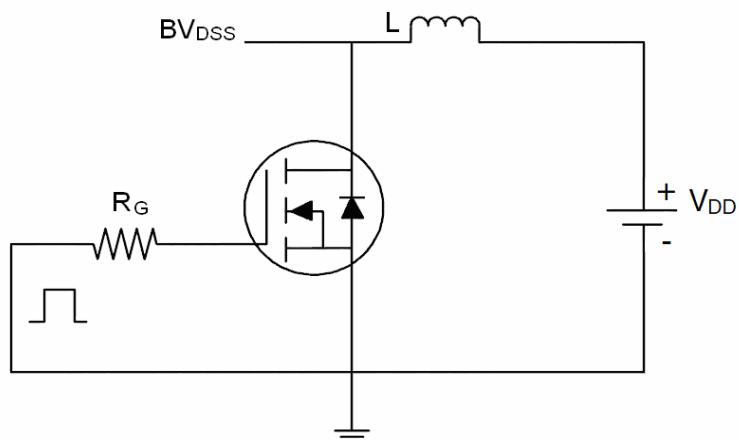
| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|--------------|--|-----|------|-----------|------------|
| Off Characteristics | | | | | | |
| Drain-Source Breakdown Voltage | BV_{DSS} | $V_{GS}=0V, I_D=250\mu A$ | 40 | 45 | - | V |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS}=40V, V_{GS}=0V$ | - | - | 1 | μA |
| Gate-Body Leakage Current | I_{GSS} | $V_{GS}=\pm 20V, V_{DS}=0V$ | - | - | ± 100 | nA |
| On Characteristics ^(Note 3) | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}=V_{GS}, I_D=250\mu A$ | 1.0 | 1.7 | 2.5 | V |
| Drain-Source On-State Resistance | $R_{DS(ON)}$ | $V_{GS}=10V, I_D=20A$ | - | 5.5 | 7 | m Ω |
| Forward Transconductance | g_{FS} | $V_{DS}=10V, I_D=20A$ | 15 | - | - | S |
| Dynamic Characteristics ^(Note4) | | | | | | |
| Input Capacitance | C_{ISS} | $V_{DS}=20V, V_{GS}=0V,$ $F=1.0MHz$ | - | 1800 | - | PF |
| Output Capacitance | C_{OSS} | | - | 280 | - | PF |
| Reverse Transfer Capacitance | C_{RSS} | | - | 190 | - | PF |
| Switching Characteristics ^(Note 4) | | | | | | |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}=20V, I_D=2A, R_L=1\Omega$ $V_{GS}=10V, R_G=3\Omega$ | - | 6.4 | - | nS |
| Turn-on Rise Time | t_r | | - | 17.2 | - | nS |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 29.6 | - | nS |
| Turn-Off Fall Time | t_f | | - | 16.8 | - | nS |
| Total Gate Charge | Q_g | $V_{DS}=20V, I_D=20A,$ $V_{GS}=10V$ | - | 29 | | nC |
| Gate-Source Charge | Q_{gs} | | - | 4.5 | | nC |
| Gate-Drain Charge | Q_{gd} | | - | 6.4 | | nC |
| Drain-Source Diode Characteristics | | | | | | |
| Diode Forward Voltage ^(Note 3) | V_{SD} | $V_{GS}=0V, I_S=10A$ | - | | 1.2 | V |
| Diode Forward Current ^(Note 2) | I_S | | - | - | 40 | A |
| Reverse Recovery Time | t_{rr} | $T_J = 25^{\circ}C, IF = 20A$ $di/dt = 100A/\mu s$ ^(Note3) | - | 29 | - | nS |
| Reverse Recovery Charge | Q_{rr} | | - | 26 | - | nC |
| Forward Turn-On Time | t_{on} | Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) | | | | |

Notes:

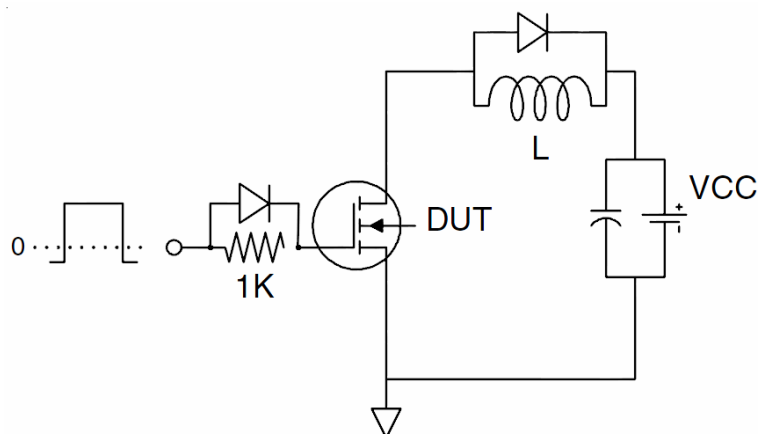
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. E_{AS} condition : $T_J=25^{\circ}\text{C}, V_{DD}=20V, V_G=10V, L=1mH, R_g=25\Omega$,

Test circuit

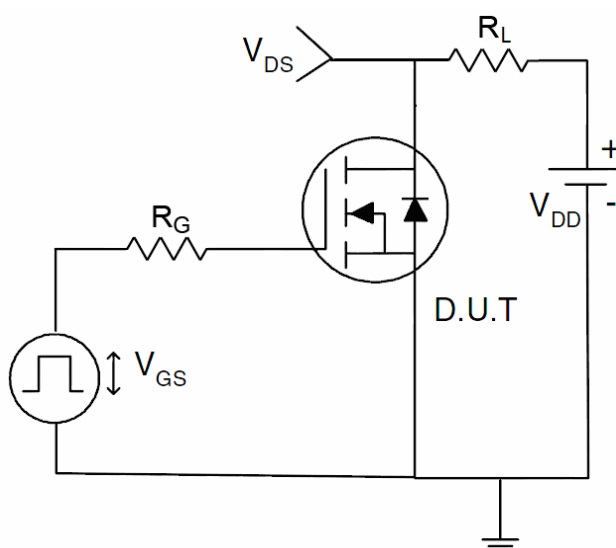
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

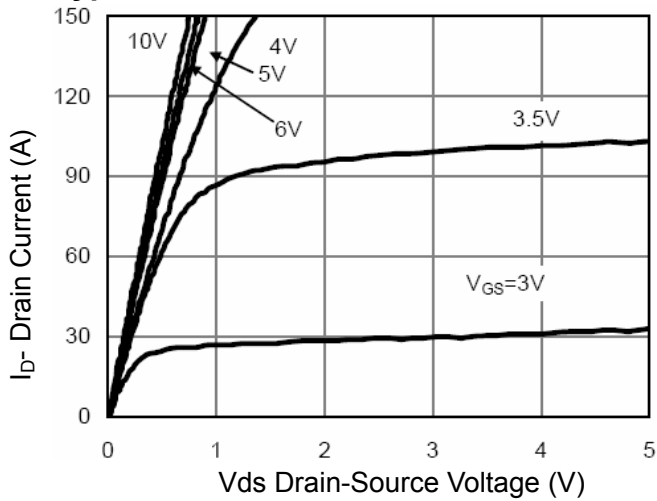


Figure 1 Output Characteristics

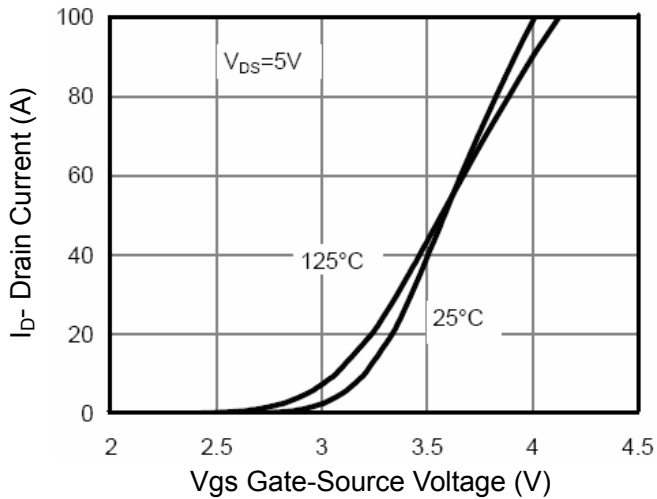


Figure 2 Transfer Characteristics

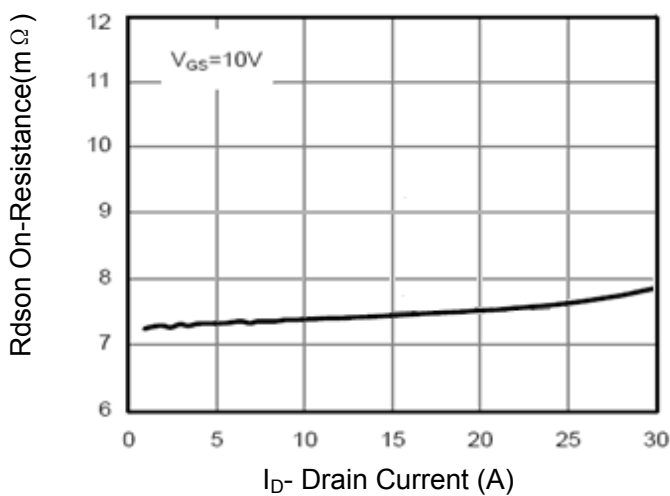


Figure 3 Rdson- Drain Current

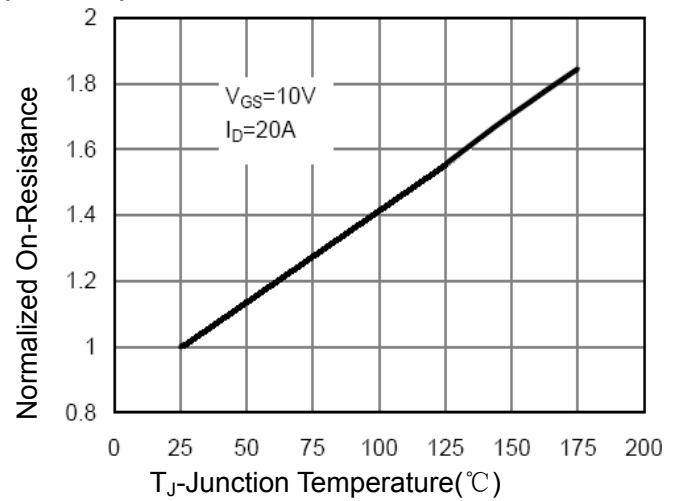


Figure 4 Rdson-Junction Temperature

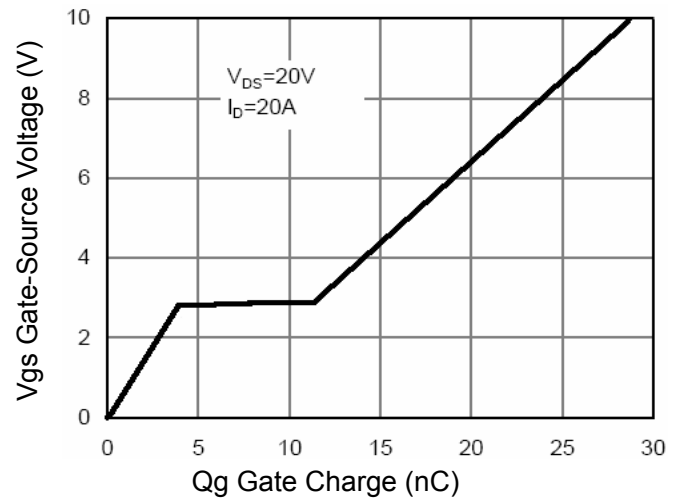


Figure 5 Gate Charge

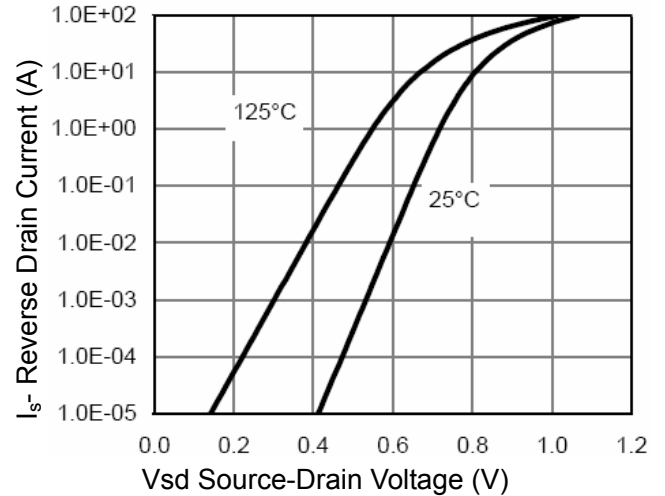


Figure 6 Source- Drain Diode Forward

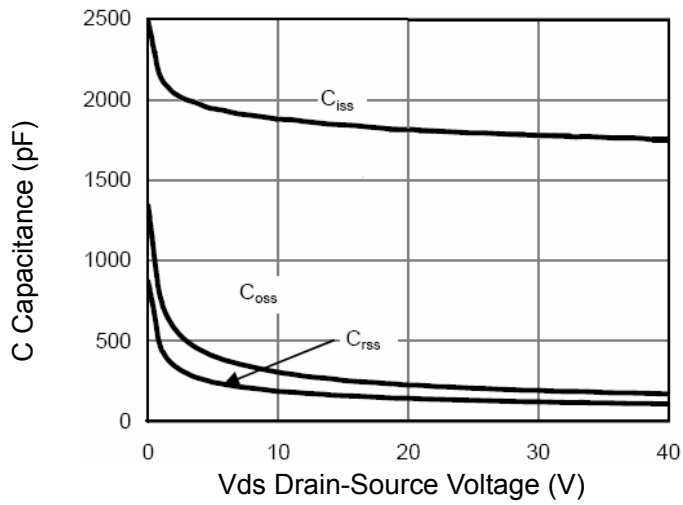


Figure 7 Capacitance vs Vds

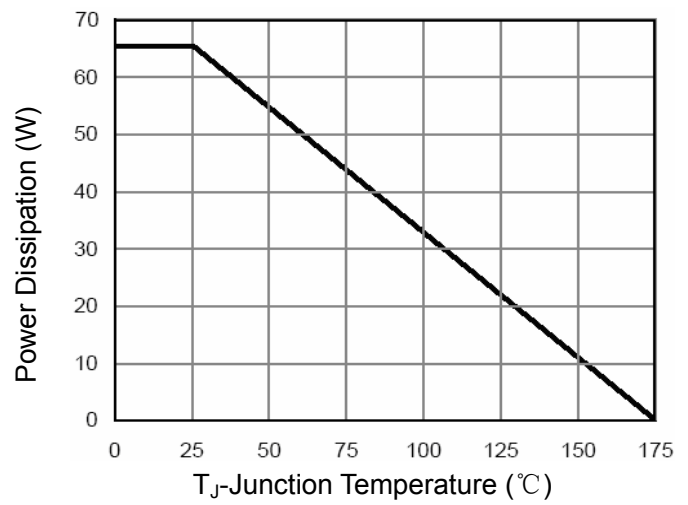


Figure 9 Power De-rating

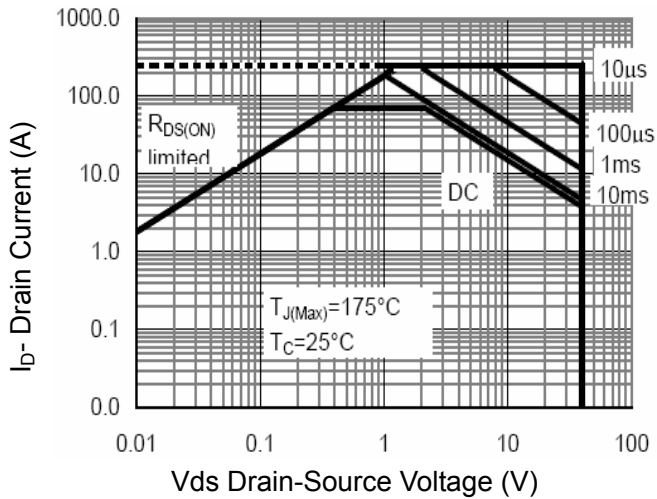


Figure 8 Safe Operation Area

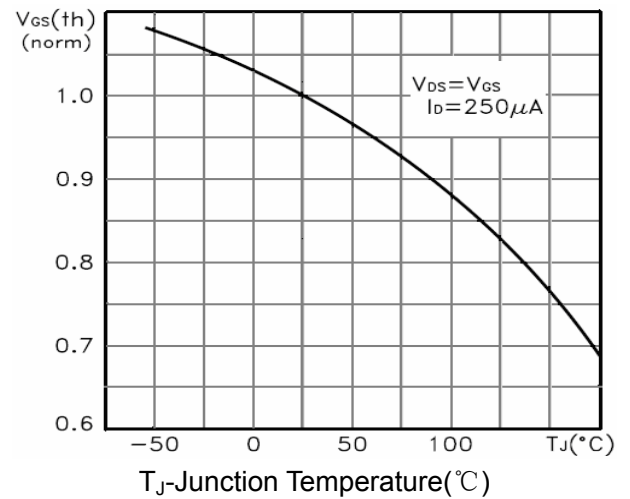


Figure 10 $V_{GS(\text{th})}$ vs Junction Temperature

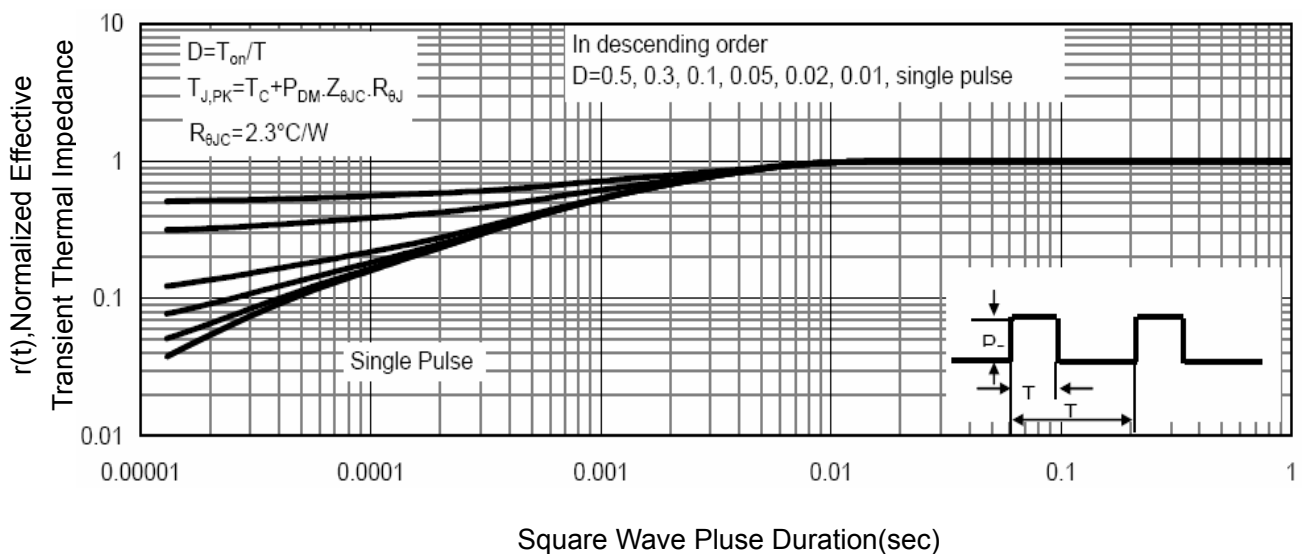
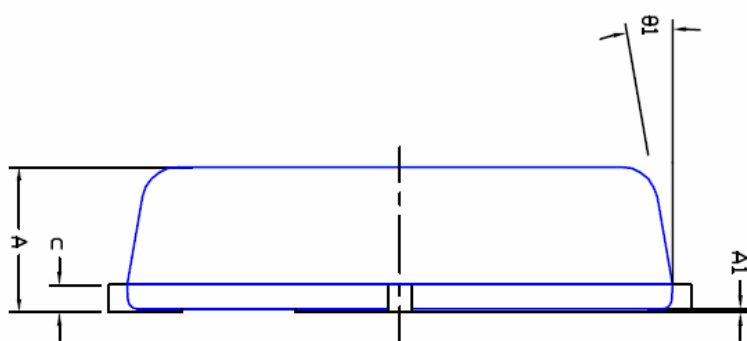
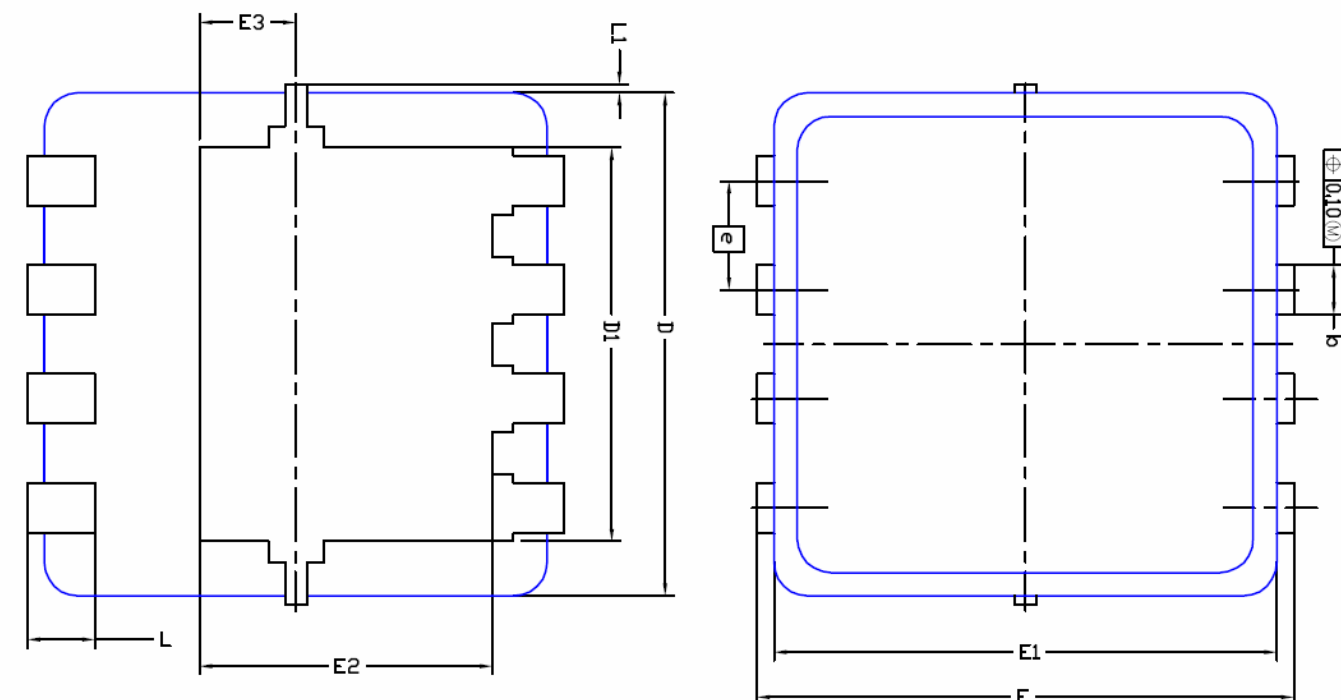


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN3X3 EP Package Information



| DIM. | MILLIMETERS | | | INCHES | | |
|------|-------------|-------|-------|-----------|--------|--------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.700 | 0.80 | 0.900 | 0.0276 | 0.0315 | 0.0354 |
| A1 | 0.00 | --- | 0.05 | 0.000 | --- | 0.002 |
| b | 0.24 | 0.30 | 0.35 | 0.009 | 0.012 | 0.014 |
| c | 0.10 | 0.152 | 0.25 | 0.004 | 0.006 | 0.010 |
| D | 3.00 BSC | | | 0.118 BSC | | |
| D1 | 2.35 BSC | | | 0.093 BSC | | |
| E | 3.20 BSC | | | 0.126 BSC | | |
| E1 | 3.00 BSC | | | 0.118 BSC | | |
| E2 | 1.75 BSC | | | 0.069 BSC | | |
| E3 | 0.575 BSC | | | 0.023 BSC | | |
| e | 0.65 BSC | | | 0.026 BSC | | |
| L | 0.30 | 0.40 | 0.50 | 0.0118 | 0.0157 | 0.0197 |
| L1 | 0 | --- | 0.100 | 0 | --- | 0.004 |
| θ1 | 0° | 10° | 12° | 0° | 10° | 12° |