

N-Channel Super Trench Power MOSFET

Description

The PT ÛFGP-Ö uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(on)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

General Features

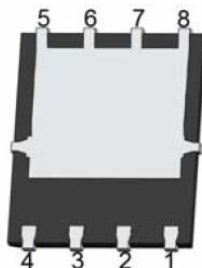
- $V_{DS} = 40V, I_D = 120A$
- $R_{DS(on)} = 2.05m\Omega$ (typical) @ $V_{GS} = 10V$
- $R_{DS(on)} = 3.1m\Omega$ (typical) @ $V_{GS} = 4.5V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating

100% UIS TESTED!
100% ΔV_{ds} TESTED!

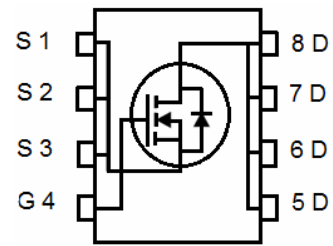
DFN 5X6



Top View



Bottom View



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
PT ÛFGP-Ö	PT ÛFGP-Ö	DFN5X6-8L	11mm	12mm	1000

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous (Silicon Limited)	I_D	120	A
Drain Current-Continuous ($T_C = 100^\circ C$)	$I_D (100^\circ C)$	84.8	A
Pulsed Drain Current (Package Limited)	I_{DM}	400	A
Maximum Power Dissipation	P_D	120	W
Derating factor		0.96	W/ $^\circ C$
Single pulse avalanche energy (Note 5)	E_{AS}	480	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	1.04	$^\circ C/W$
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Electrical Characteristics (T_C=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	40		-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics <small>(Note 3)</small>						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	1.2	1.7	2.2	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =60A	-	2.05	2.35	mΩ
		V _{GS} =4.5V, I _D =60A	-	3.1	3.6	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V,I _D =60A		56	-	S
Dynamic Characteristics <small>(Note4)</small>						
Input Capacitance	C _{iss}	V _{DS} =20V,V _{GS} =0V, F=1.0MHz	-	2250	-	PF
Output Capacitance	C _{oss}		-	815	-	PF
Reverse Transfer Capacitance	C _{rss}		-	43	-	PF
Switching Characteristics <small>(Note 4)</small>						
Turn-on Delay Time	t _{d(on)}	V _{DD} =20V,I _D =60A V _{GS} =10V,R _G =1.6Ω	-	9	-	nS
Turn-on Rise Time	t _r		-	3.5	-	nS
Turn-Off Delay Time	t _{d(off)}		-	30	-	nS
Turn-Off Fall Time	t _f		-	4	-	nS
Total Gate Charge	Q _g	V _{DS} =20V,I _D =60A, V _{GS} =10V	-	44		nC
Gate-Source Charge	Q _{gs}		-	7.5		nC
Gate-Drain Charge	Q _{gd}		-	7		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} =0V,I _S =60A	-		1.2	V
Diode Forward Current	I _S		-	-	120	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = I _S di/dt = 100A/μs <small>(Note3)</small>	-		21	nS
Reverse Recovery Charge	Q _{rr}		-		60	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition : T_J=25°C, V_{DD}=20V, V_G=10V, L=0.5mH, R_G=25Ω

Typical Electrical and Thermal Characteristics

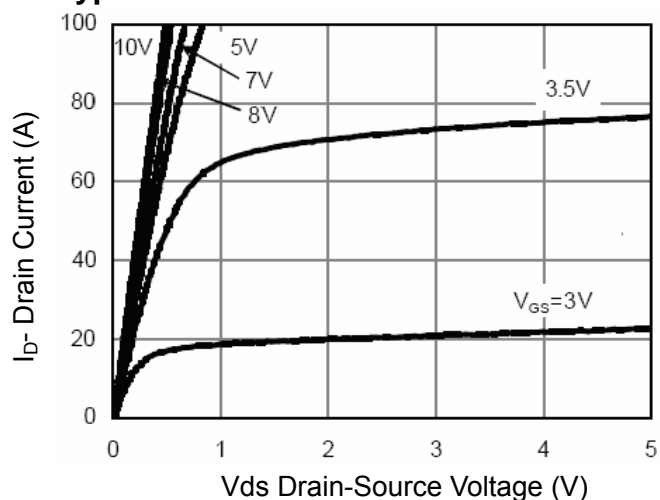


Figure 1 Output Characteristics

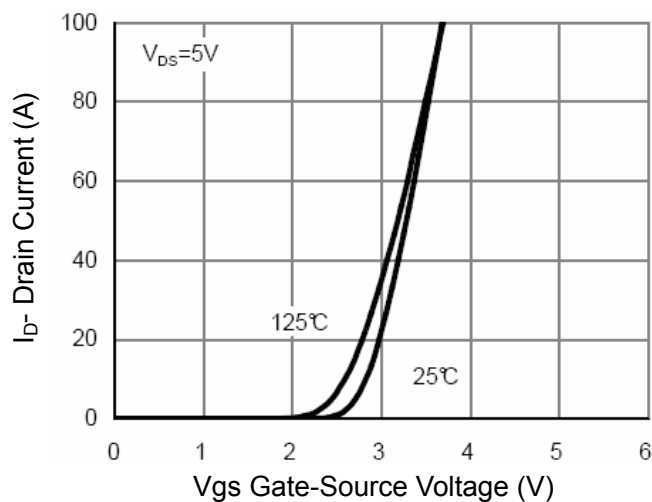


Figure 2 Transfer Characteristics

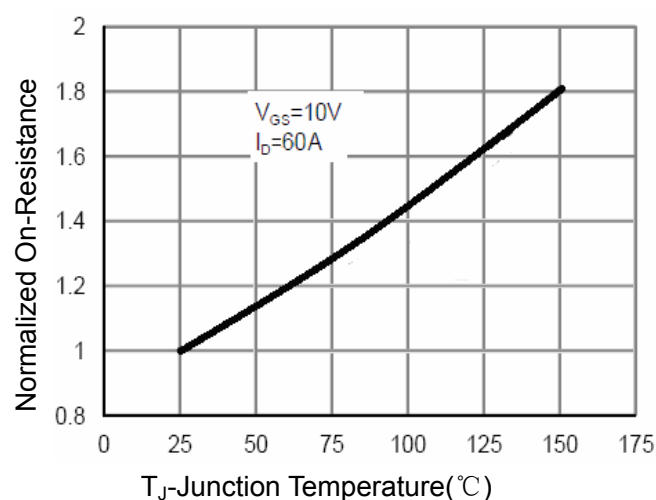


Figure 4 $R_{DS(on)}$ -Junction Temperature

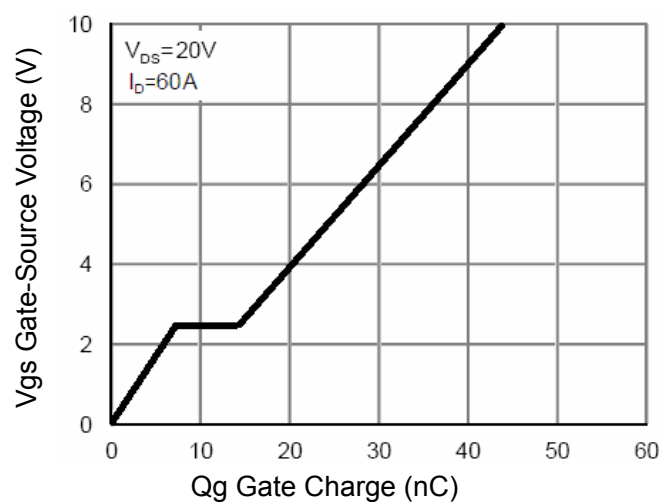


Figure 5 Gate Charge

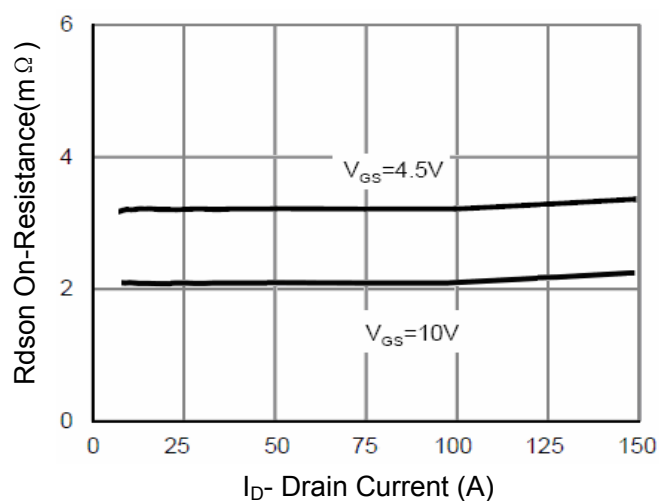


Figure 3 $R_{DS(on)}$ - Drain Current

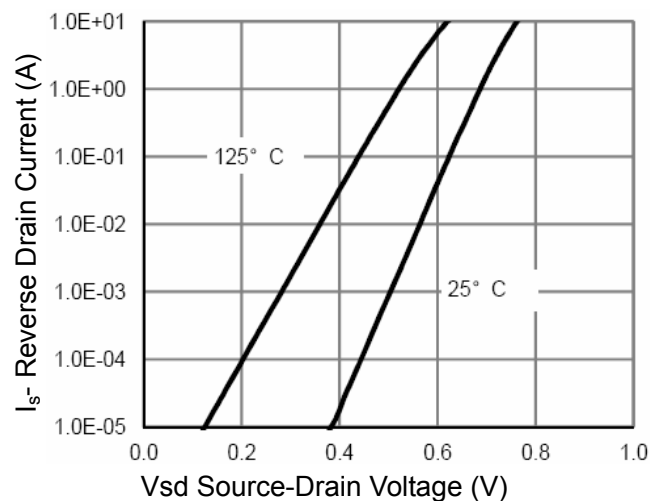


Figure 6 Source- Drain Diode Forward

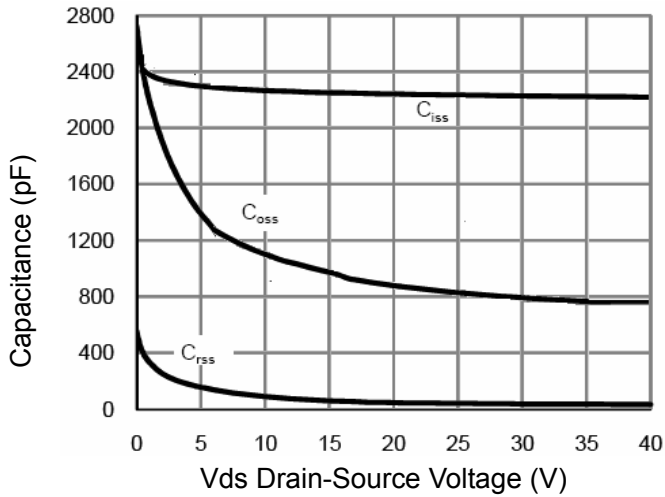


Figure 7 Capacitance vs Vds

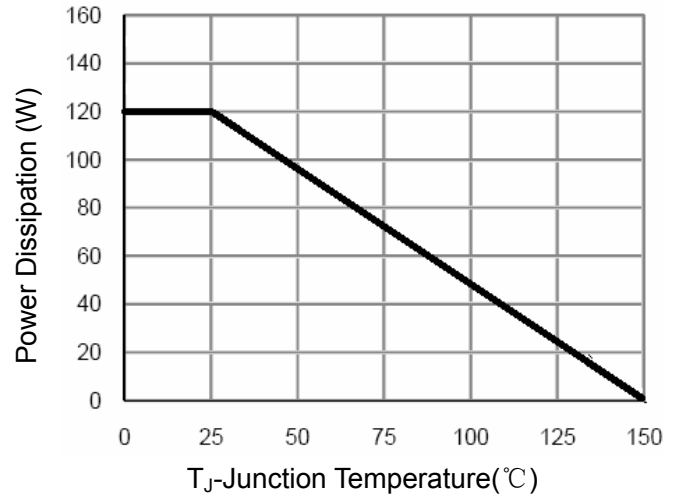


Figure 9 Power De-rating

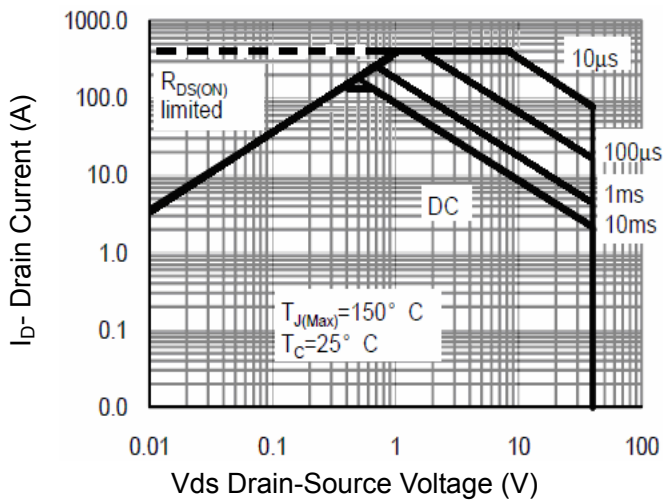


Figure 8 Safe Operation Area

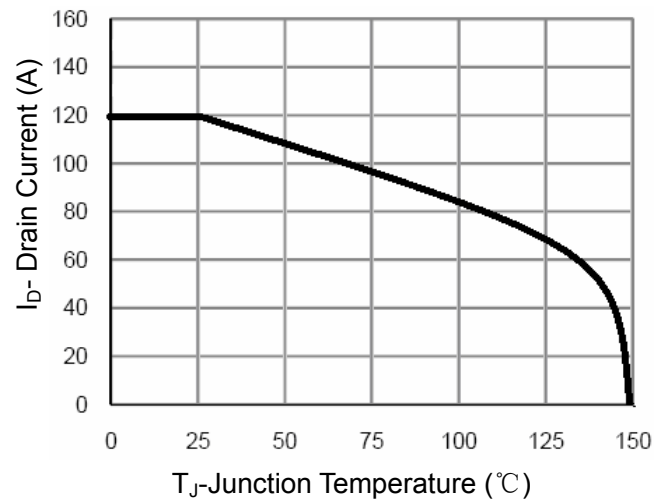


Figure 10 Current De-rating

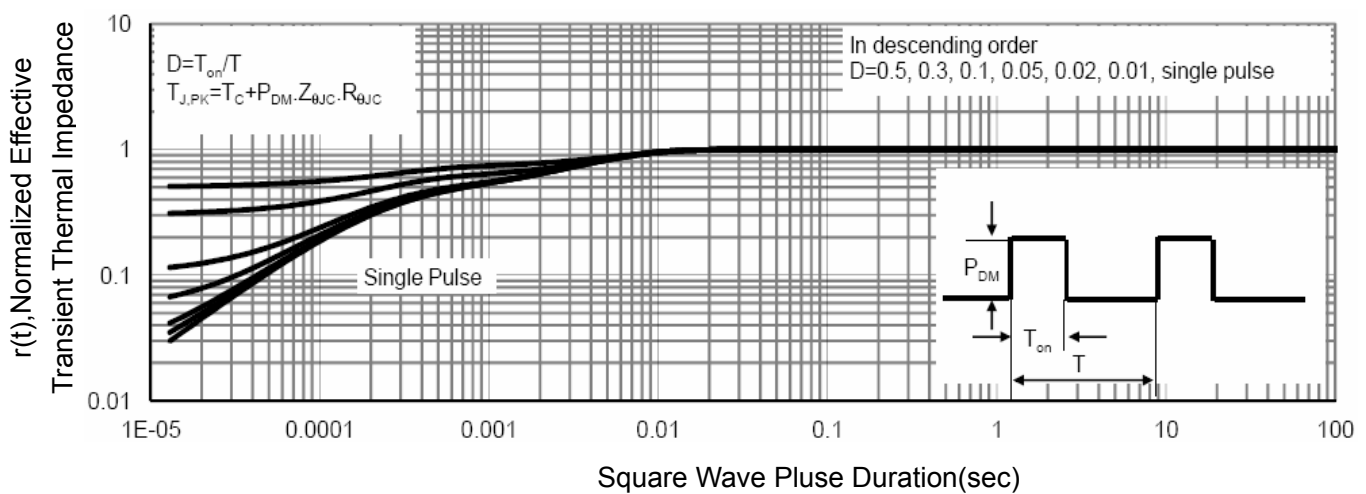


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package Information

