

## P-Channel Enhancement Mode Power MOSFET

### Description

The HM4421D uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. This device is well suited for high current load applications.

### General Features

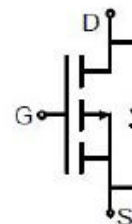
- $V_{DS} = -60V, I_D = -14A$   
 $R_{DS(ON)} < 25m\Omega @ V_{GS} = -10V$
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation

### Application

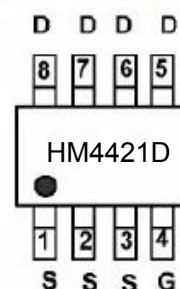
- Load switch

**100% UIS TESTED!**

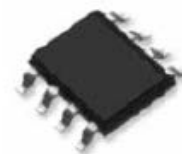
**100%  $\Delta V_{ds}$  TESTED!**



Schematic diagram



Marking and pin Assignment



SOP-8 top view

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HM4421D	HM4421D	SOP8	-	-	-

### Absolute Maximum Ratings ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	-14	A
Drain Current-Continuous( $T_C = 100^\circ\text{C}$ )	$I_D(100^\circ\text{C})$	-9.8	A
Pulsed Drain Current	$I_{DM}$	-42	A
Maximum Power Dissipation	$P_D$	95	W
Derating factor		0.76	W/ $^\circ\text{C}$
Single pulse avalanche energy (Note 5)	$E_{AS}$	722	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ\text{C}$

### Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	1.31	$^\circ\text{C/W}$
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**Electrical Characteristics ( $T_c=25^{\circ}\text{C}$  unless otherwise noted)**

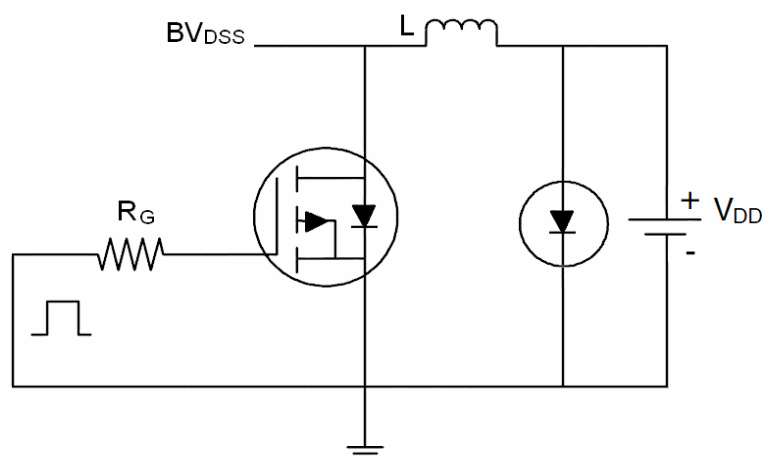
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =-250μA	-60	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-60V,V <sub>GS</sub> =0V	-	-	-1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V,V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics <sup>(Note 3)</sup>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> ,I <sub>D</sub> =-250μA	-2	-2.6	-3.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-10A	-	20	25	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =-10V,I <sub>D</sub> =-10A	-	25	-	S
Dynamic Characteristics <sup>(Note4)</sup>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =-25V,V <sub>GS</sub> =0V, F=1.0MHz	-	6460	-	PF
Output Capacitance	C <sub>OSS</sub>		-	719	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	535	-	PF
Switching Characteristics <sup>(Note 4)</sup>						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =-30V, R <sub>L</sub> =1.5Ω, V <sub>GS</sub> =-10V,R <sub>G</sub> =3Ω	-	15	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	17	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	40	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	45	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-30,I <sub>D</sub> =-10A, V <sub>GS</sub> =-10V	-	75		nC
Gate-Source Charge	Q <sub>gs</sub>		-	16		nC
Gate-Drain Charge	Q <sub>gd</sub>		-	19		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <sup>(Note 3)</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V,I <sub>S</sub> =-10A	-		-1.2	V
Diode Forward Current <sup>(Note 2)</sup>	I <sub>S</sub>		-	-	-20	A
Reverse Recovery Time	t <sub>rr</sub>	TJ = 25°C, IF =- 10A	-	50		nS
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = -100A/μs(Note3)	-	59		nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

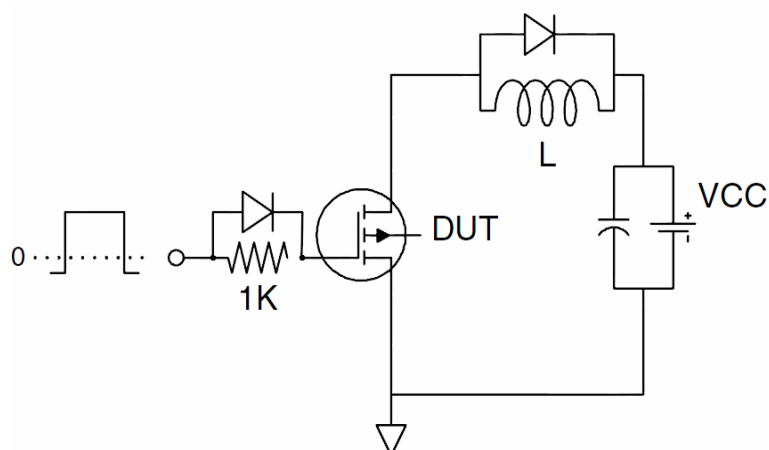
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5.  $E_{AS}$  condition:  $T_J=25^{\circ}\text{C}, V_{DD}=-20V, V_G=-10V, L=1mH, R_g=25\Omega, I_{AS}=38A$

## Test Circuit

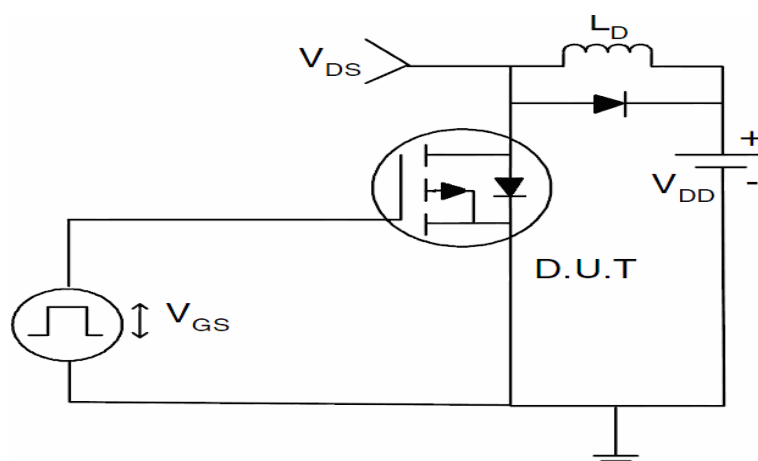
### 1) $E_{AS}$ Test Circuit



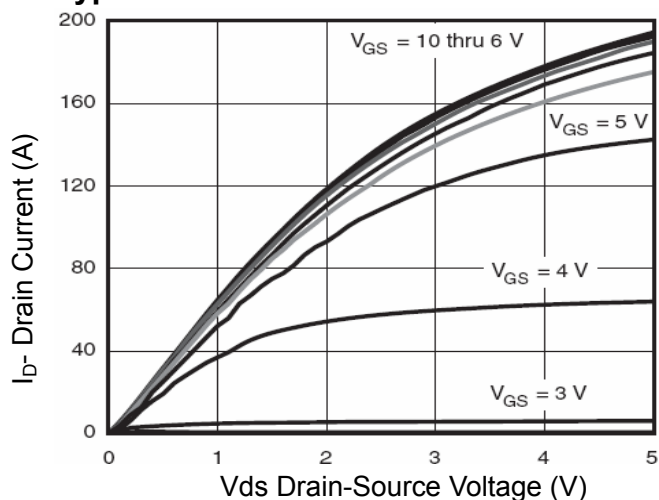
### 2) Gate Charge Test Circuit



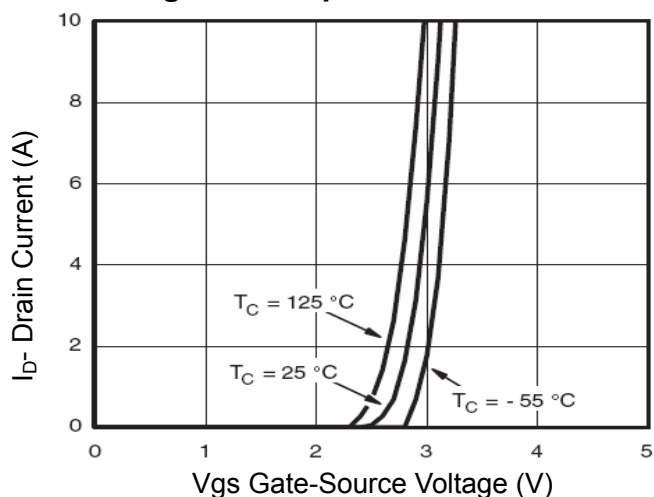
### 3) Switch Time Test Circuit



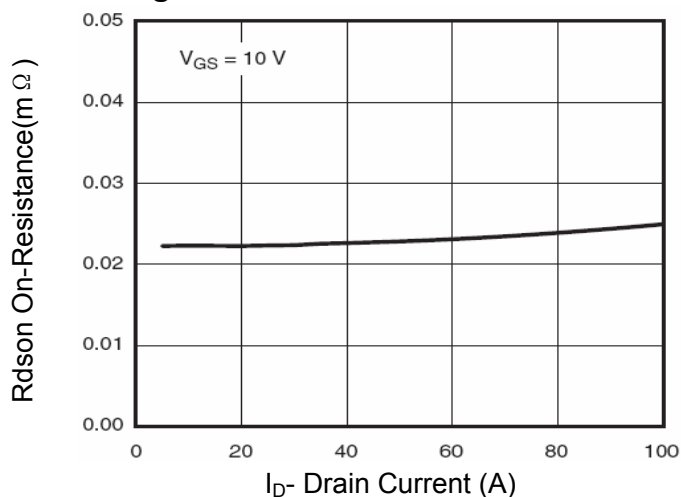
# Typical Electrical and Thermal Characteristics (Curves)



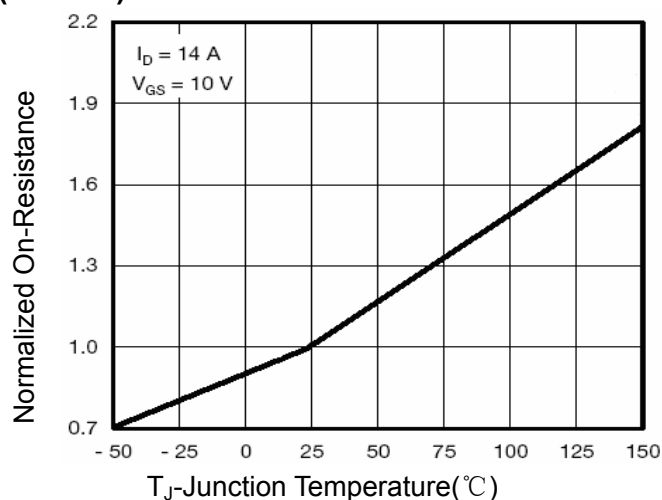
**Figure 1 Output Characteristics**



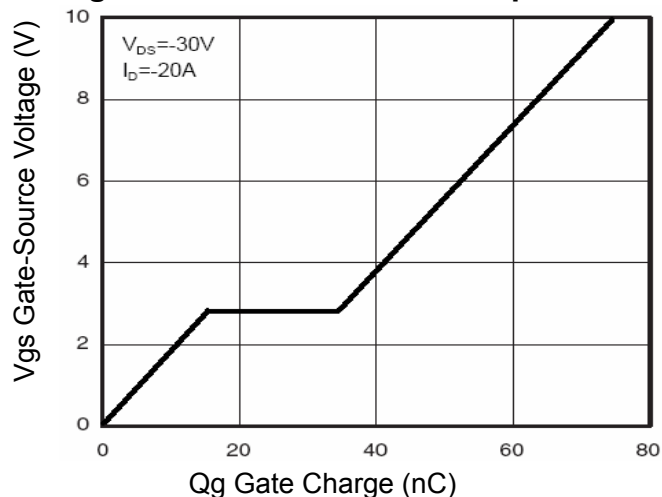
**Figure 2 Transfer Characteristics**



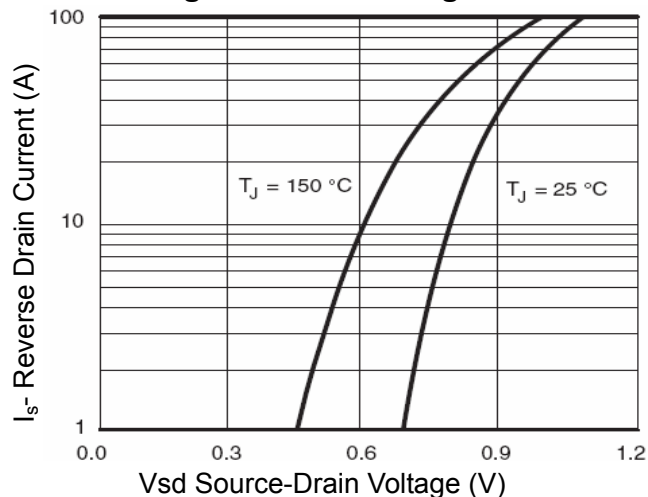
**Figure 3 Rdson- Drain Current**



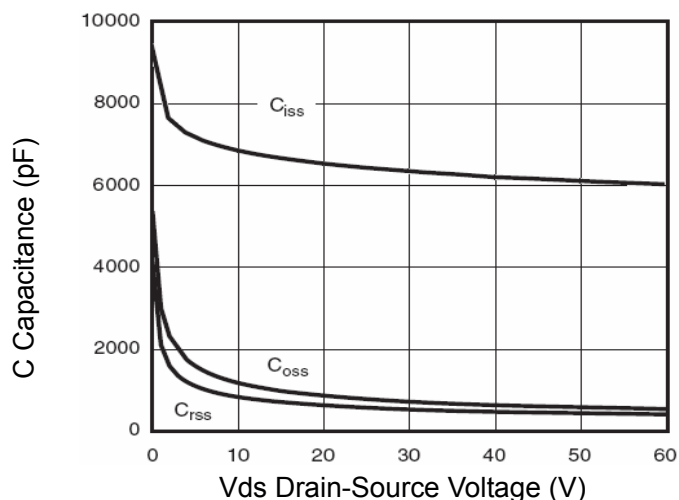
**Figure 4 Rdson-Junction Temperature**



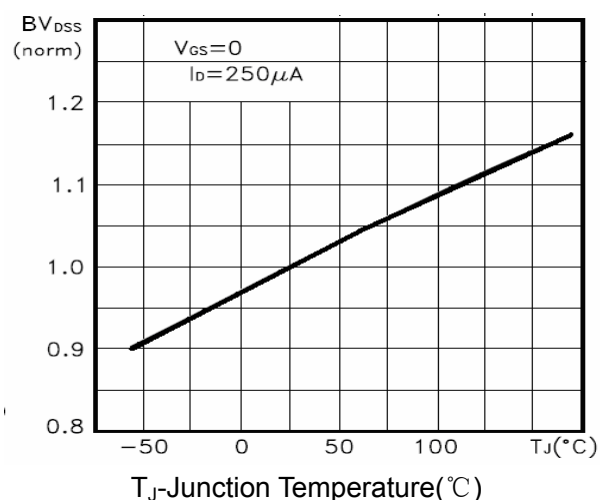
**Figure 5 Gate Charge**



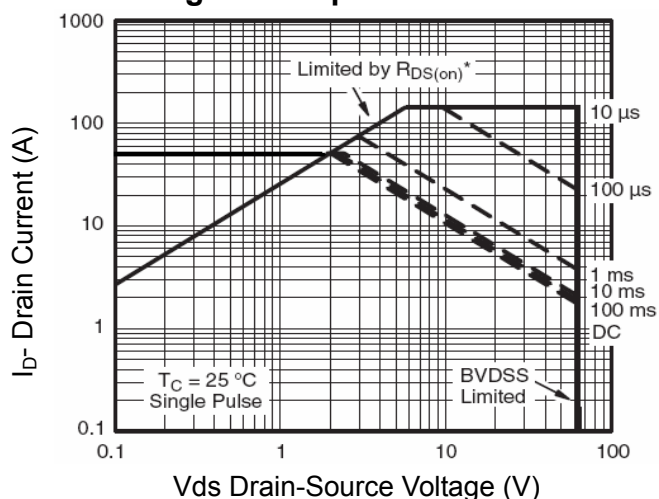
**Figure 6 Source- Drain Diode Forward**



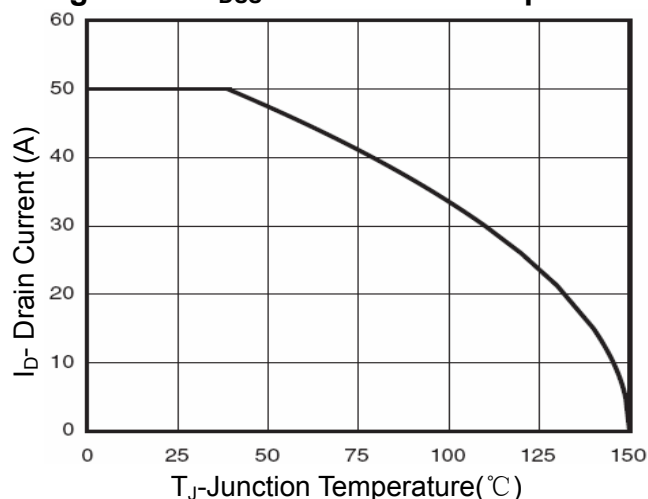
**Figure 7 Capacitance vs Vds**



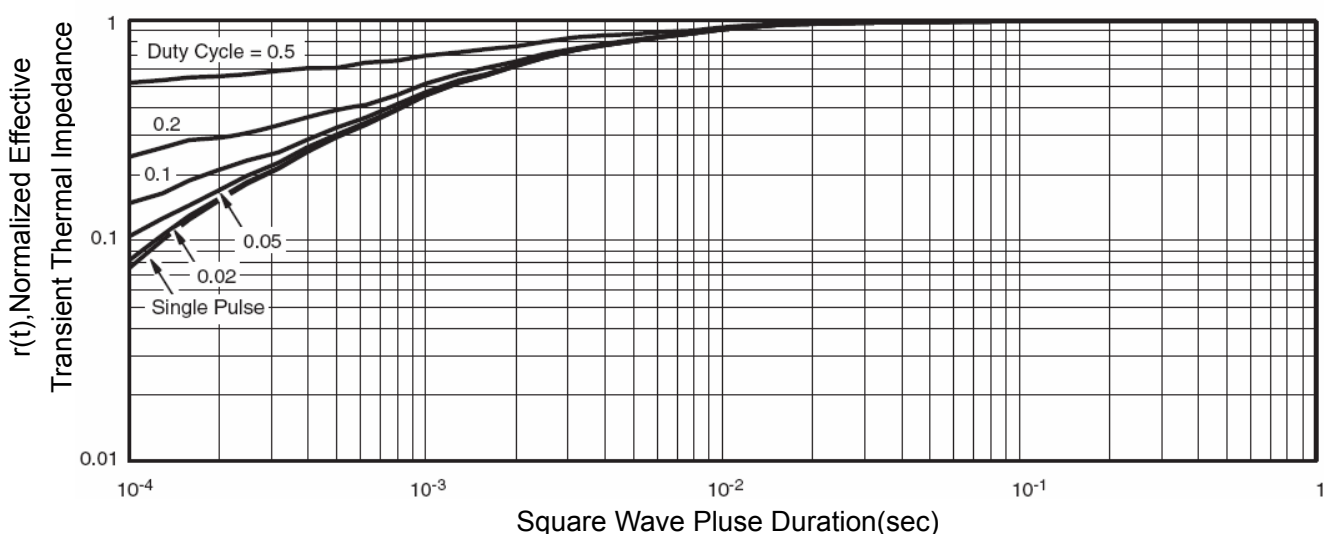
**Figure 9  $BV_{DSS}$  vs Junction Temperature**



**Figure 8 Safe Operation Area**

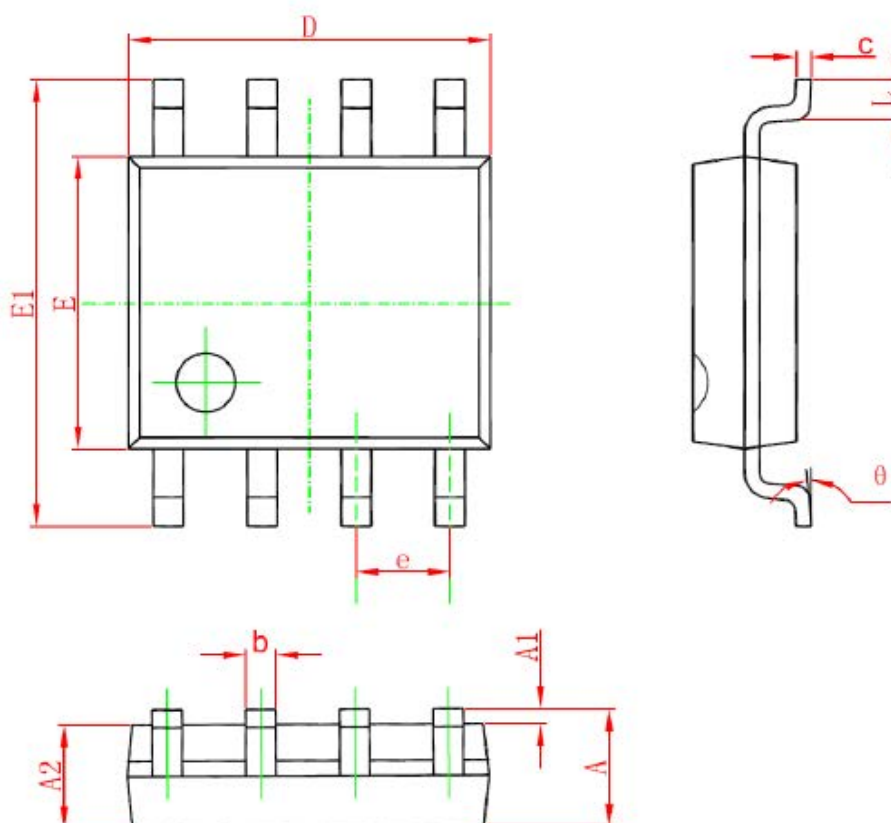


**Figure 10  $I_D$  Current Derating vs Junction Temperature**



**Figure 11 Normalized Maximum Transient Thermal Impedance**

# SOP-8 PACKAGE IN FORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	0.483 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

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